Dragonchip

APPNOTE034

System migration from DC6688FL32A/B to DC6688FLE / FLX

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Table of Content

1 Introduction

The Objective of this document is to provide the DC6688FL32A/B user on how to migrate to DC6688FLX / DC6688FLE.

2 Notes on firmware migration

Item		Description
A	Timer 0 and Timer 1 setting	the following condition at the same time happened is invalid: i) Timer 1 set to mode 1, and ii) Timer 0 set to mode 2

B	Add instructions	Add the following instructions to the beginning of the program
		 MOV R0,#PFS
		 MOV A,#PROG_SIZE
		 MOVX @R0,A

For item B, if Program Flash memory required in DC6688FLX/DC6688FLE is 24KB, same as DC6688FL32A/B, then no need to set this 'PFS' register in program. In this case, the ratio of Program Flash/Data Flash memory in DC6688FL64X / FL64E, as an example, is 24KB/39.5KB after migration. For DC6688FL96E, the ratio is 24KB/71KB.

If the size of Program Flash memory is no longer 24KB, this 'PFS' register have to add at the beginning of the program as shown below.

```
        ORG     002BH

        RETI

;-------------------------------------
; Main Program
;-------------------------------------
STARTUP:
;-------------------------------------
; define option here
; user is prohibited to modify it
#ifndef CHIP
        MOV     0A0H,#0
#endif
        ;---------------------------
        ; delay 100ms to let power stable
        ; in case the firmware write data flash at the beginning
        CALL    DELAY

        ;---------------------------
        ; initialize the program/data flash size at the very beginning of program,
        ; Warning: these instructions should be located in program memeory within 0x0000 ~ 0x0200
        MOV     R0,#PFS
        MOV     A,#PROG_SIZE
        MOVX    @R0,A
        ;---------------------------
```

3 Further Notes on Firmware

This section applies to DC6688FL32A/FLB/DC6688FLX/FLE.

Item	Description
a	Initialization Data for Data Flash memory
b	Add 100ms delay at the beginning of the program
c	Initialization for SRAM
d	Counter A should be reset after exit from stop mode

For item a, to avoid using firmware to initialize Data Flash memory during in production line, it is recommended to also download the image to data flash memory by SL or SPI programming.

For item b, this applies to case where factory do initialization on data flash memory in production line by firmware itself. In view of the unstable power supply in production line found at the instant of insertion, add this delay at the beginning of the program to let the power stable before starting to run the firmware in production line.

An example on item b is shown below inside the red rectangle:

```
; Main Program
;----------------------------------------
STARTUP:
;----------------------------------------
; define option here
; user is prohibited to modify it
#ifndef CHIP
        MOV     0A0H,#0
#endif
        ;---------------------------
        ; if immigrate from DC6688FL32A to DC6688FL16B-E, the following should be added
        MOV     R0,#0FH
        MOV     A,#00111111B
        MOVX    @R0,A

        MOV     R0,#PCCONL
        MOVX    A,@R0
        ORL     A,#11000000B
        MOVX    @R0,A

        ;---------------------------
        ; delay 100ms to let power stable
        ; in case the firmware write data flash at the beginning
        CALL    DELAY

        ;---------------------------
```

For item c, this is a must as on power up, the contents in the SRAM are undetermined.
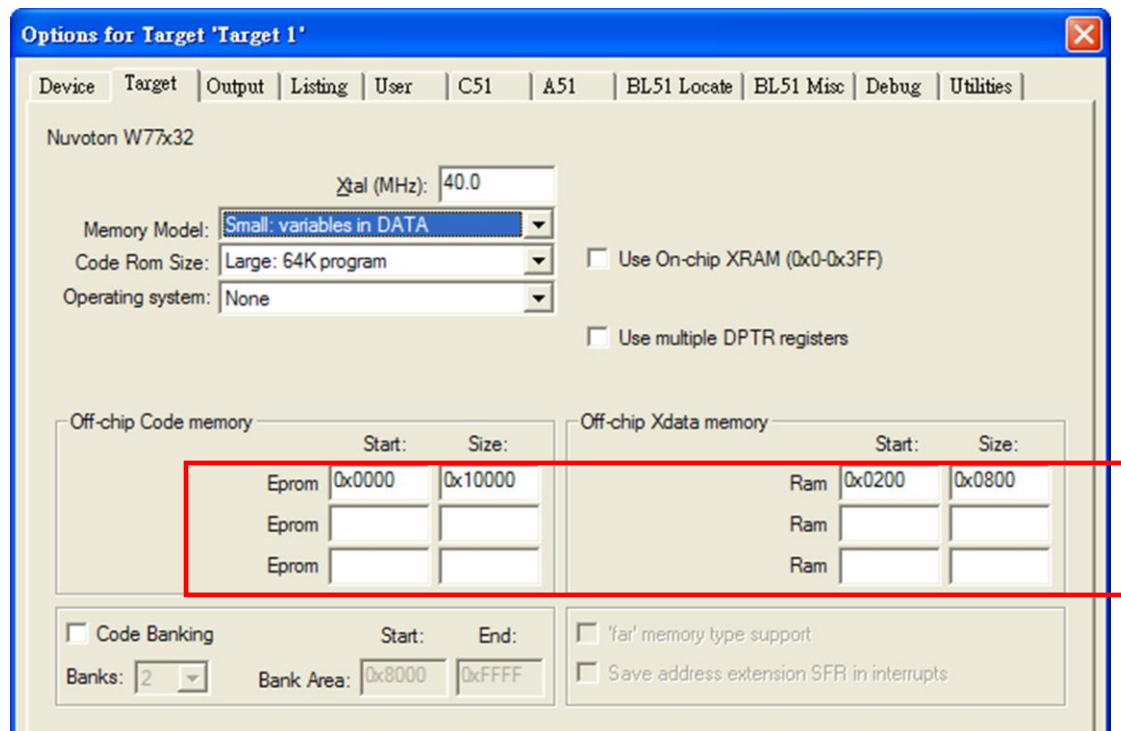
4 Keil Compiler's environment

4.1 DEEMAX emulator

4.1.1 Migrating to DC6688FLX / FL64E

DC6688FL96E do not applicable.

When using emulator, there are some instructions, listed below, that the When migrating the firmware from DC6688FL32A/B to DC6688FLX / FL64E, some settings in Keil compiler have to modify as shown below highlighted in red box.

4.2 DC6688EMT-4T emulator

4.2.1 Migrating to DC6688FLX / FLE

Make use of our software "Source Code Template" to generate the template for FLX / FLE. Copy all the settings in Keil to your existing project. Settings refer to the section "Keil Project Settings" in the manual of emulator.

5 DEEMAX emulator

It only applies to:
1) DC6688FL32A/B
2) DC6688FLX
3) DC6688FL64E (FL96E do not apply)

It is suggested to use DC6688EMT-4T emulator for DC6688FLE as described in section 6.

5.1 Limitation on DC6688FL32A/B

Before listing the limitation on DC6688FLX, we go through on DC6688FL32A/B.

When using emulator, there are some instructions, listed below, that the machine cycle is not identical to that used in our chip.

|	Dragonchip	DEEMAX emulator
Mnemonic	Machine cycle	Machine cycle
RET	4	2
RETI	4	2
JMP @A+DPTR	3	2
MOVC A,@A+DPTR	3	2
MOVC A,@A+PC	3	2
INC DPTR	3	2

Additional limitation:
1. Power down mode is not implemented in ICE, don't use it, otherwise, undetermined result occurs.
2. No ISP select pin on CON4 in the ICE
3. No XOUT pin on CON4 in the ICE
4. No pull-up resistors in the ICE's port A, B and C
5. No watchdog (basic timer)
6. No backup mode
7. No ISP programming
8. No UART0[1], UART1
9. Only operated at 3.3V power
10. No access to 'T1_PCNTA' register
11. No T2 output on PC2 by setting bit 'T2OE' in 'T2MOD' register

Remarks:
[1] UART0[1] is only not available in "Development board for DC6688F16LC

ver1.0"

Item 4 above is suggested to add an optional pull-up resistor (as shown below) on customer's target board.
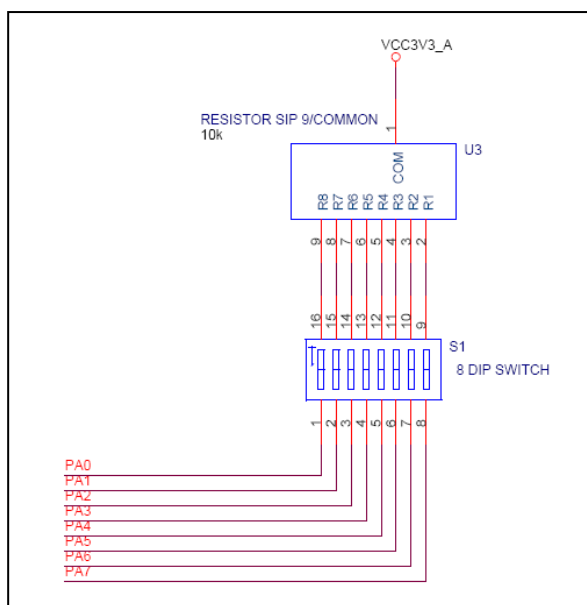
The Dip switch serves as an enable switch when connecting to emulator, and a disable switch when connecting to IC.

5.2 Limitation on DC6688FLX

Basically, the limitation on DC6688FL64X is identical to DC6688FL32A/B. Therefore, section 5.1 also applies here, plus the following.

Those who developed DC6688FL32A/B are suggested to follow the steps below:
1) develop using emulator for DC6688FL32A/B
2) download the firmware to IC(DC6688FL32A/B), and check the prototype.
3) Develop using emulator for DC6688FLX
4) download the firmware to IC(DC6688FLX), and check the prototype.

Item 2 above make sure that the major functions work properly
The major function includes:
1) CPU
2) 256B-SRAM
3) 512B-SRAM
4) Data flash memory
5) Learning (hardware(IRI pin, T24 timer) + software library(AppNote011))

The difference between DC6688FL32A/B and DC6688FLX is only on:
1) The ratio of program flash/data flash size.

Part No.	Program flash	Data flash

DC6688FL32A/B	24KB	8KB
DC6688FL48X	24KB	24KB
DC6688FL64X	24KB	39.5KB

2) Expanded SRAM size

Part No.	Size
DC6688FL32A/B	512B
DC6688FL48X/FL64X	2048B

5.3 Limitation on DC6688FL64E

Basically, the limitation on DC6688FL64E is identical to DC6688FL64X.
Therefore, section 5.2 also applies here, plus the following.
1. No I2C
2. No SPI
3. Fractional Divider as baud-rate generator for UART0 not available

Those who developed DC6688FL32A/B are suggested to follow the steps below:
1) develop using emulator for DC6688FL32A/B
2) download the firmware to IC(DC6688FL32A/B), and check the prototype.
3) Develop using emulator for DC6688FLX
4) download the firmware to IC(DC6688FL64E), and check the prototype.

Item 2 above make sure that the major functions work properly
The major function includes:
1) CPU
2) 256B-SRAM
3) 512B-SRAM
4) Data flash memory
5) Learning (hardware(IRI pin, T24 timer) + software library(AppNote011))

The difference between DC6688FL32A/B and DC6688FL64E is only on:
1) The ratio of program flash/data flash size.

Part No.	Program flash	Data flash
DC6688FL32A/B	24KB	8KB
DC6688FL64E	24KB	39.5KB

2) Expanded SRAM size
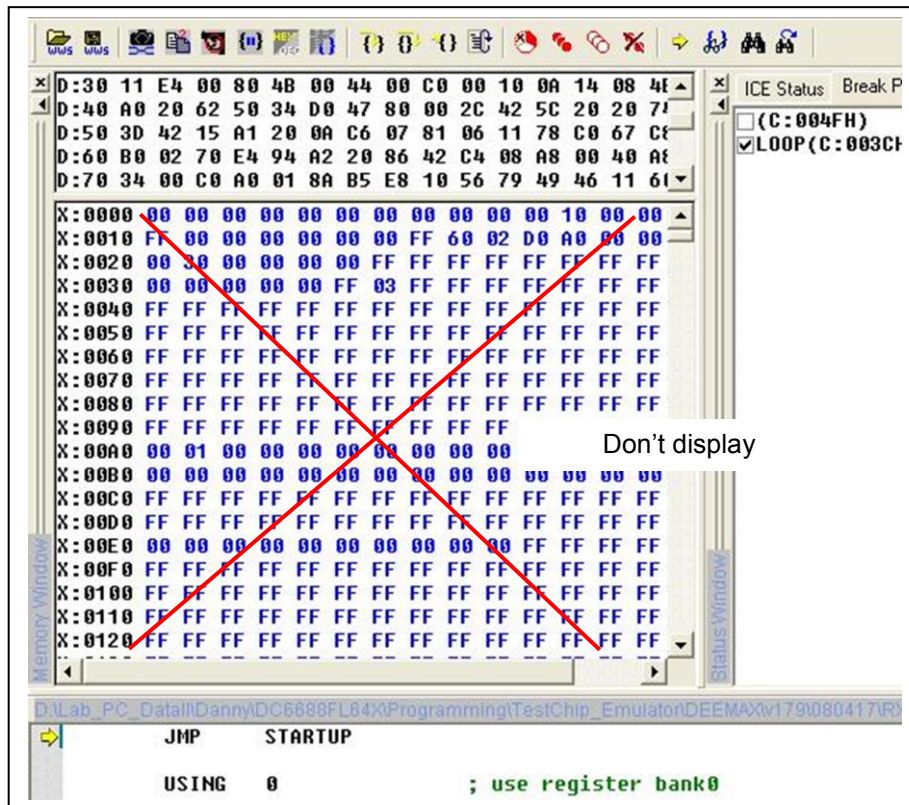
Part No.	Size
DC6688FL32A/B	512B
DC6688FL64E	2048B

5.4 Precaution on using the Emulator

When debugging the program in emulator, in the period of using the following register:
1) "RACTL" = 0x01 or 0x03
2) "RBCTL" = 0x01 or 0x03
Display of the memory region X:0000H ~ 01FFH is prohibited as shown below:

Since when setting "RACTL" to 0x01, whenever reading/writing "RDBA" the pointer "RAPTH/RAPTL" will automatically increment by 1. The emulator itself, in order to update the "Memory window", will also read the whole XFR table one time whenever the program stops running. This reading will disturb the pointer "RAPTH/RAPTL" and the program to get the wrong data. This principle also applies to "RBCTL"

Display of the memory region X:0200H ~ FFFFH is allowed.

5.5 Environment setting

In the DEEMAX emulator's software environment, the 'Memory map' in 'Status window' has to modify as shown below:
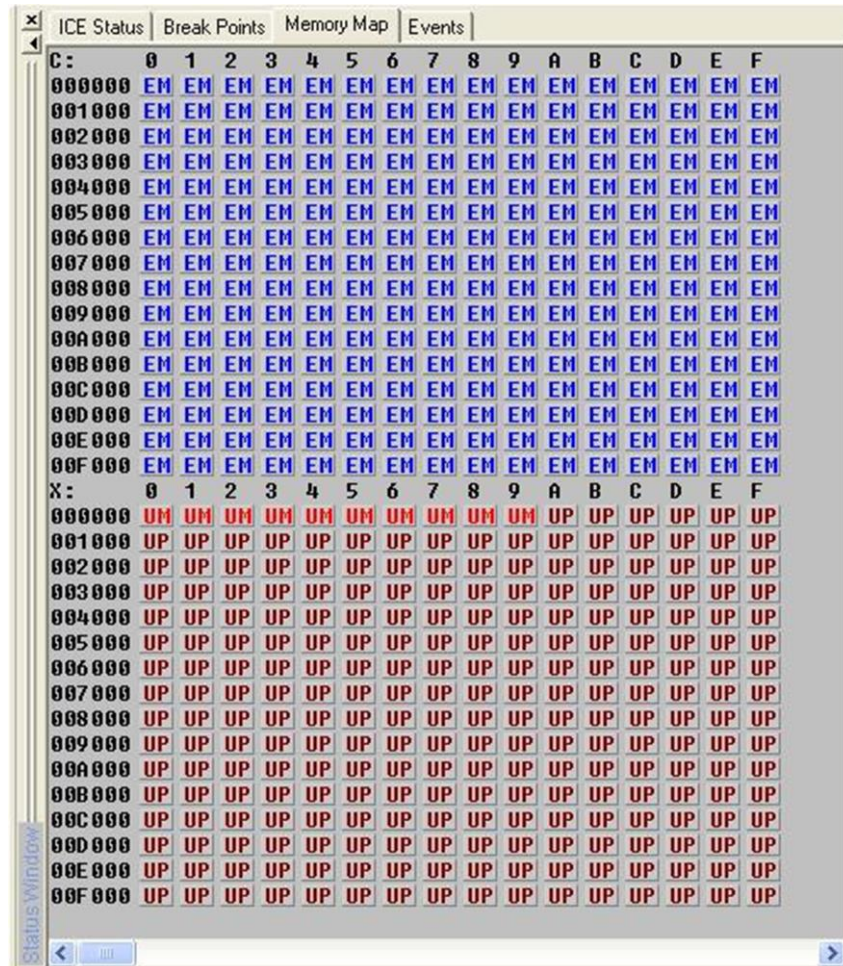
6 DC6688EMT-4T emulator

It only applies to:
1) DC6688FL32A/B
2) DC6688FLX
3) DC6688FLE

6.1 Limitation

Detail refers to the manual of emulator.

Those who developed DC6688FL32A/B are suggested to follow the steps below:
1) develop using emulator for DC6688FL32A/B
2) download the firmware to IC(DC6688FL32A/B), and check the prototype.
3) Develop using emulator for DC6688FLX/FLE
4) download the firmware to IC(DC6688FLX/FLE), and check the prototype.

Item 2 above make sure that the major functions work properly
The major function includes:
1) CPU
2) 256B-SRAM
3) 512B-SRAM
4) Data flash memory
5) Learning (hardware(IRI pin, T24 timer) + software library(AppNote011))

The difference between DC6688FL32A/B and DC6688FLE is only on:
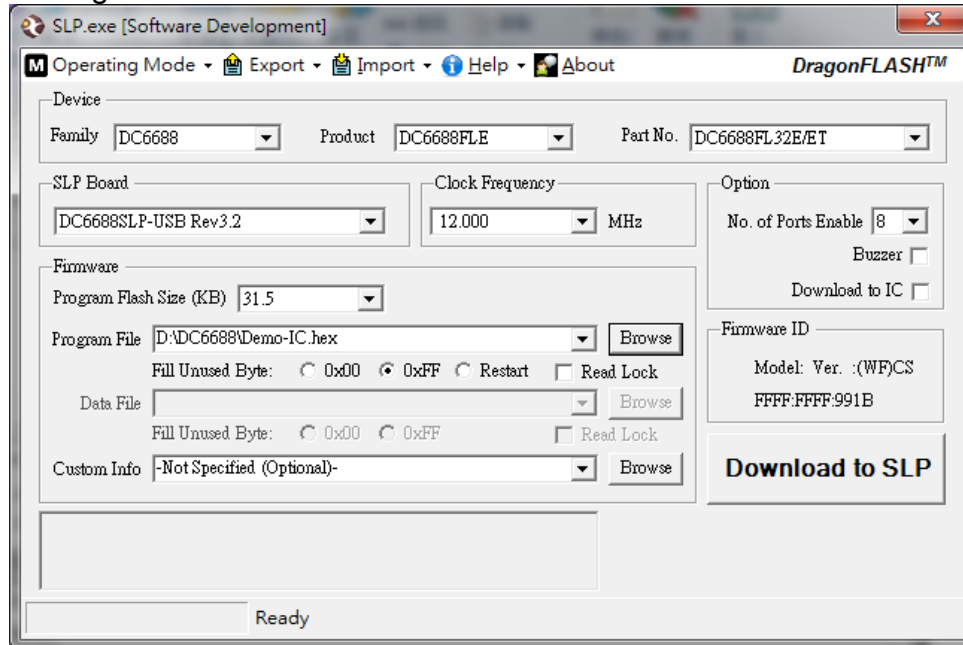1) The ratio of program flash/data flash size.

Part No.	Program flash	Data flash
DC6688FL32A/B	24KB	8KB
DC6688FL48X	24KB	24KB
DC6688FL64X/FL64E	24KB	39.5KB
DC6688FL96E	24KB	71KB

2) Expanded SRAM size

Part No.	Size
DC6688FL32A/B	512B
DC6688FL48X/FL64X/FL64E/FL96E	2048B

7 Software SLP

Settings in Software SLP for DC6688FL32E is shown below:

Revision History

Document Rev. No.	Issued Date	Section	Page	Description	Edited By	Reviewed By
1.0	Apr, 2008			Preliminary		
1.1	Apr, 2008			Revised section 5.2 and 5.3		
1.2	June, 2008			Revise page 1 and section 2		
1.3	Oct, 2011	All		Add DC6688FL32B	Danny Ho	Celia Ki
		4		Diagram update		
1.4	May, 2012	4.2, 6		Add DC6688FLE	Danny Ho	Celia Ki
1.5	Apr, 2013	4, 5, 6		Add DC6688FL64E and update DC6688EMT-4T emulator information	Danny Ho	Celia Ki
1.6	Nov, 2015	7		Added Software SLP description	Danny Ho	Celia Ki

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