Dragonchip

DC6388EMT
User Manual

User Manual of DC6388EMT
Emulator for DC6388F Family

User Manual
Document Revision 1.3 Nov, 2017

Contents

1 Introduction

This document briefly describes the details of the development tool 'Emulator for DC6388F Family (DC6388EMT)'.

1.1 Supported Products

Part Number	Supported Products
DC6388EMT-FD	DC6388FD

1.2 Package

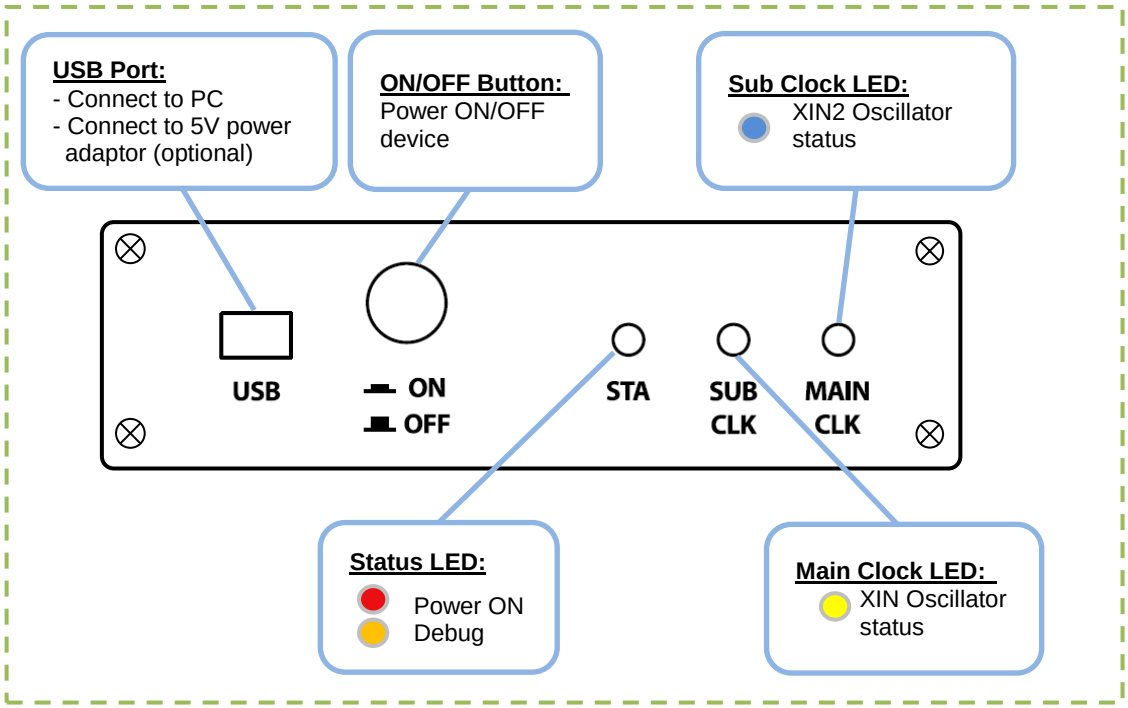
1) Emulator
2) Power Adaptor (5VDC Output)
3) Mini USB Cable
4) User Manual
5) Installation CD

1.3 Useful Links

1) DC6388EMT Emulator
   http://www.dragonchip.com/TechDoc/DC6388F/DevTools/EMT.htm
2) DC6388F Technical Website
   http://www.dragonchip.com/TechDoc/DC6388.htm

2 Hardware

2.1 Control Interface



2.2 IDE Connector

Connect the emulator to target board through the ribbon cable and IDE Connector. Put a 2.54mm pitch (52P / 64P) box header or pin header on the target board. The connector pin assignments are listed below:

48-pin package

Connector Pin No.	MCU Pin No.	Pin Name	Connector Pin No.	MCU Pin No.	Pin Name
1	12	PE2	2	11	PE1
3	13	PE3	4	10	PE0
5	14	PE4	6	-	-
7	15	PE5	8	-	-
9	-	-	10	-	-
11	17	PE6	12	9	PD4/SEG28
13	18	PE7	14	8	PD3/SEG27
15	-	-	16	7	PD2/SEG26
17	-	-	18	6	PD1/SEG25
19	21	VSS	20	5	PD0/SEG24
21	-	-	22	4	PB7/SEG23
23	23	VDD	24	3	PB6/SEG22
25	24	PC1	26	2	PB5/SEG21
27	-	-	28	1	PB4/SEG20
29	25	COM0	30	48	PB3/SEG19
31	26	COM1	32	47	PB2/SEG18
33	27	COM2	34	46	PB1/SEG17
35	28	COM3	36	45	PB0/SEG16
37	29	SEG0/V3	38	44	PA7/SEG15
39	30	SEG1/V2	40	43	PA6/SEG14
41	31	SEG2/V1	42	42	PA5/SEG13
43	32	SEG3	44	41	PA4/SEG12
45	33	SEG4	46	40	PA3/SEG11
47	34	SEG5	48	39	PA2/SEG10
49	35	SEG6	50	38	PA1/SEG9
51	36	SEG7	52	37	PA0/SEG8
53	-	-	54	-	-
55	-	-	56	-	-

57	-	-	58	-	-
59	-	-	60	-	-
61	-	-	62	-	-
63	-	-	64	-	-

52-pin package

Connector Pin No.	MCU Pin No.	Pin Name	Connector Pin No.	MCU Pin No.	Pin Name
1	1	PE2	2	52	PE1
3	2	PE3	4	51	PE0
5	3	PE4	6	50	PD7/SEG31
7	4	PE5	8	49	PD6/SEG30
9	-	-	10	48	PD5/SEG29
11	6	PE6	12	47	PD4/SEG28
13	7	PE7	14	46	PD3/SEG27
15	-	-	16	45	PD2/SEG26
17	-	-	18	44	PD1/SEG25
19	10	VSS	20	43	PD0/SEG24
21	-	-	22	42	PB7/SEG23
23	12	VDD	24	41	PB6/SEG22
25	13	PC1	26	40	PB5/SEG21
27	-	-	28	39	PB4/SEG20
29	15	COM0	30	38	PB3/SEG19
31	16	COM1	32	37	PB2/SEG18
33	17	COM2	34	36	PB1/SEG17
35	18	COM3	36	35	PB0/SEG16
37	19	SEG0/V3	38	34	PA7/SEG15
39	20	SEG1/V2	40	33	PA6/SEG14
41	21	SEG2/V1	42	32	PA5/SEG13
43	22	SEG3	44	31	PA4/SEG12
45	23	SEG4	46	30	PA3/SEG11
47	24	SEG5	48	29	PA2/SEG10
49	25	SEG6	50	28	PA1/SEG9
51	26	SEG7	52	27	PA0/SEG8
53	-	-	54	-	-
55	-	-	56	-	-
57	-	-	58	-	-
59	-	-	60	-	-
61	-	-	62	-	-
63	-	-	64	-	-

64-pin package

Connector Pin No.	MCU Pin No.	Pin Name	Connector Pin No.	MCU Pin No.	Pin Name
1	17	PE2	2	16	PE1
3	18	PE3	4	15	PE0
5	19	PE4	6	11	PD7/SEG39
7	20	PE5	8	10	PD6/SEG38
9	-	-	10	9	PD5/SEG37
11	22	PE6	12	8	PD4/SEG36
13	23	PE7	14	7	PD3/SEG35
15	-	-	16	6	PD2/SEG34
17	-	-	18	5	PD1/SEG33
19	26	VSS	20	4	PD0/SEG32
21	-	-	22	3	PB7/SEG31
23	28	VDD	24	2	PB6/SEG30
25	29	PC1	26	1	PB5/SEG29
27	-	-	28	64	PB4/SEG28

29	35	SEG0/COM4	30	63	PB3/SEG27
31	36	SEG1/COM5	32	62	PB2/SEG26
33	37	SEG2/COM6	34	61	PB1/SEG25
35	38	SEG3/COM7	36	60	PB0/SEG24
37	40	SEG4/V3	38	59	PA7/SEG23
39	41	SEG5/V2	40	58	PA6/SEG22
41	42	SEG6/V1	42	57	PA5/SEG21
43	43	SEG7	44	56	PA4/SEG20
45	44	SEG8	46	55	PA3/SEG19
47	45	SEG9	48	54	PA2/SEG18
49	46	SEG10	50	53	PA1/SEG17
51	47	SEG11	52	52	PA0/SEG16
53	48	SEG12	54	34	COM3
55	49	SEG13	56	33	COM2
57	50	SEG14	58	32	COM1
59	51	SEG15	60	31	COM0
61	12	PC0	62	39	V4
63	13	PC2	64	14	PC3

Note:
1) The voltage supply to emulator chip is 3.3V (VDD pin voltage). User should do emulation at this voltage level only.
2) Backup mode (LVR triggered) would not be supported.
3) Low voltage indicator (LVI) would not be supported.
4) LVD enable pin VDCE would not be supported
5) Programming pin ISPSEL would not be supported
6) Reset pin RSTN would not be supported.
7) XIN, XOUT, XIN2 and XOUT2 would not be supported. Instead, there are on-board oscillators to supply clocks and the settings can be configured in DragonICE.

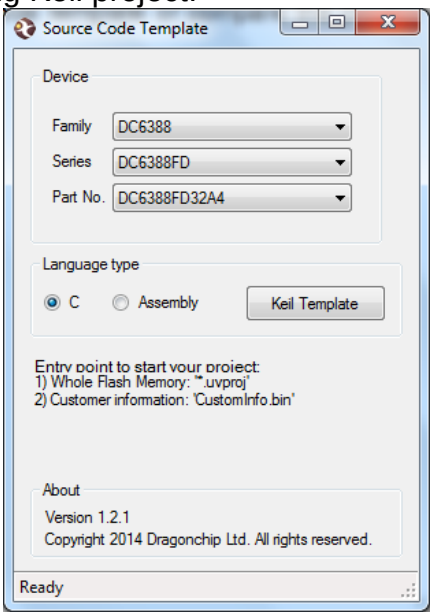
3 Software Installation

Install the following components
1) Keil PK51 Professional Developers Kit (v9.05 or later)
2) Dragonchip development tools package ‘DC_TOOL_Rev2.5.9.exe’ or later:
    a. Source Code Template
    b. DragonICE Driver
    c. Software SLP

Note: After installing the DragonICE driver, connect the emulator to PC USB port, the driver will be installed automatically. In case the PC fails to locate the driver, select the driver path “C:\WINDOWS\system32” manually.

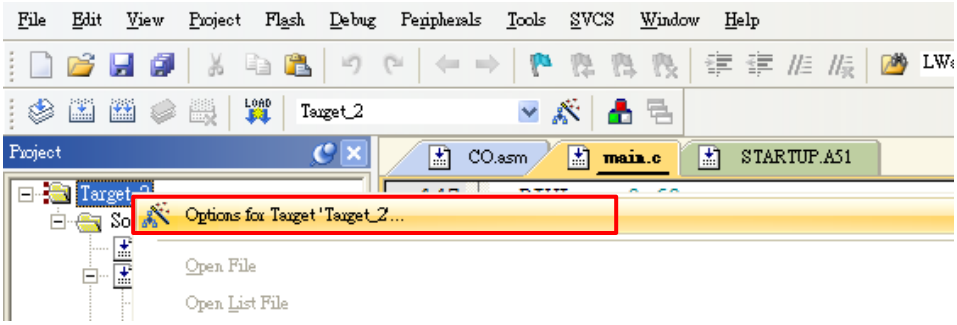
3.1 Source Code Template

This software can help to generate Keil project templates for various products with all necessary project settings for using emulators. User can either start the development with the generated source code template or compare the project settings with their existing Keil project.

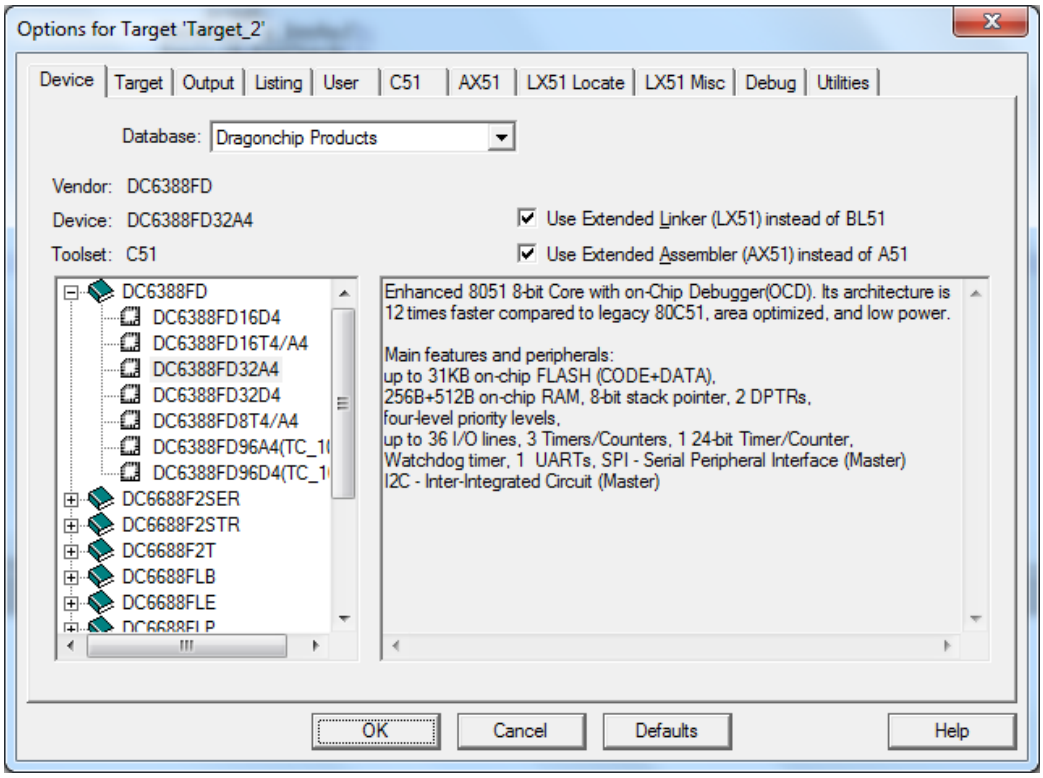


3.2 Keil Project Settings

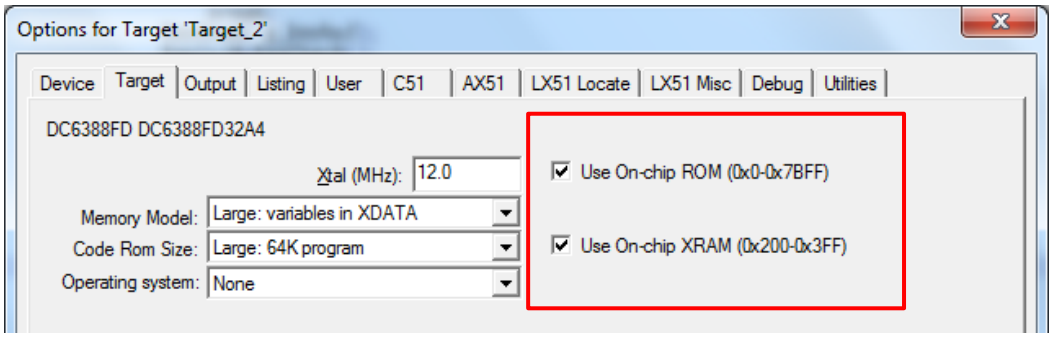
1) Enter 'Options for Target'



2) ‘Device’ Tab - Select DC6388 part number from the list.

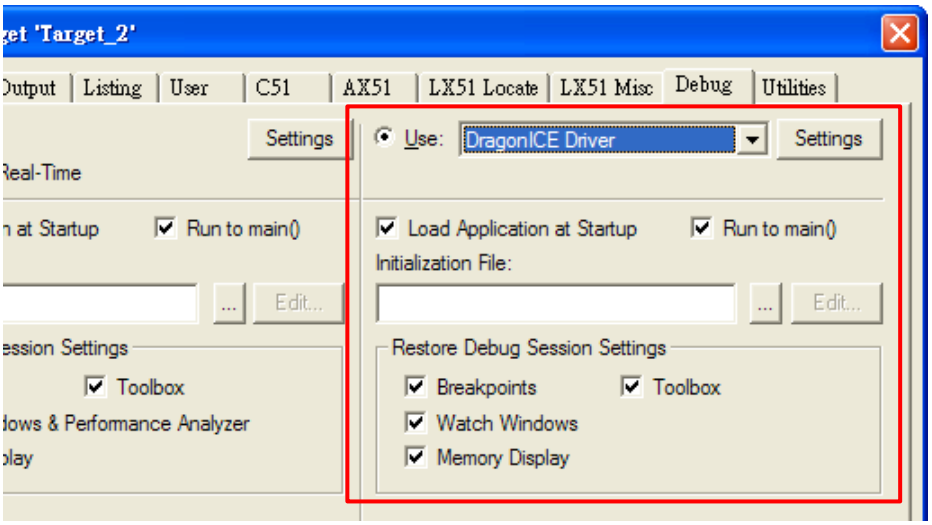


3) ‘Target’ Tab – Always check the 2 boxes for ROM and XRAM setting.

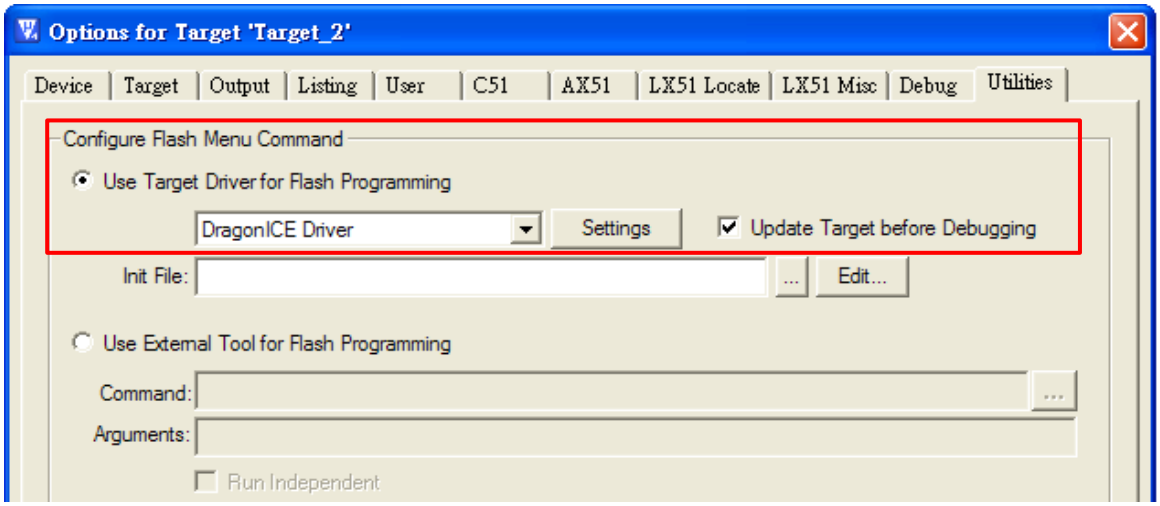


Note: The Clock frequency in this page is invalid setting. The setting should be selected in ‘Programming Setting’ instead.

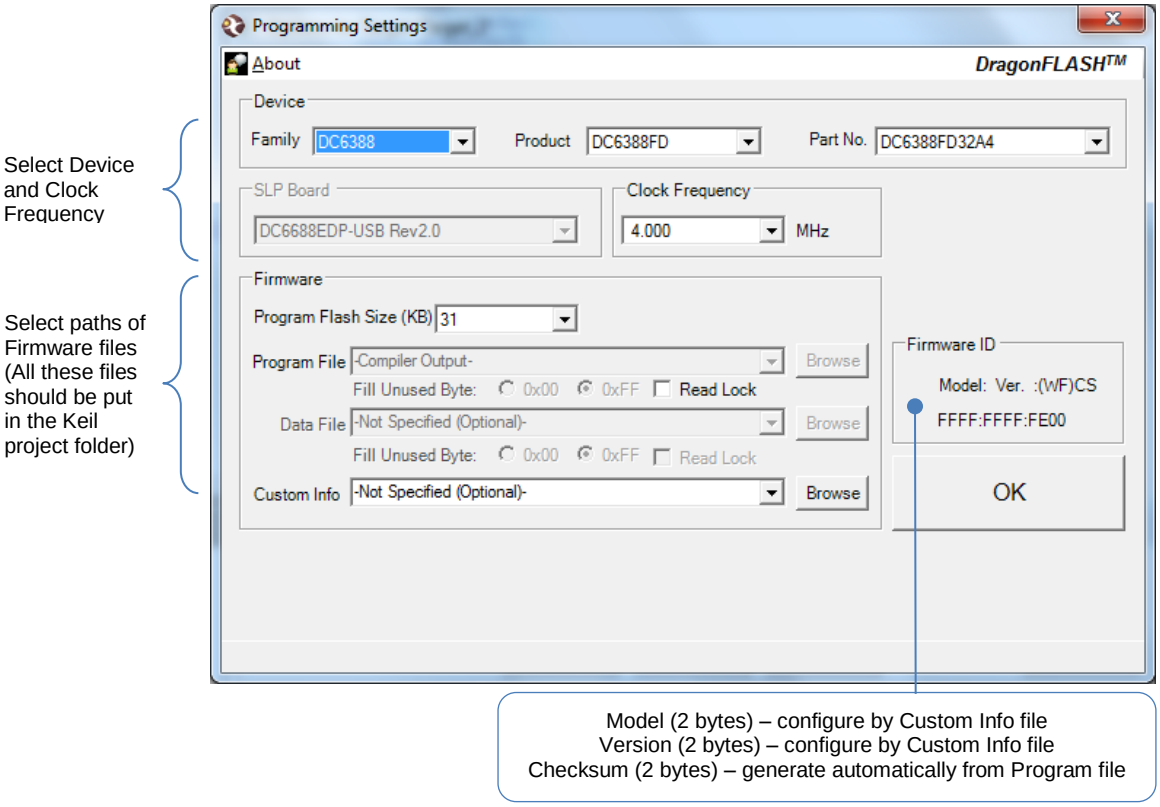
4) ‘Debug’ Tab - Follow the settings shown below:



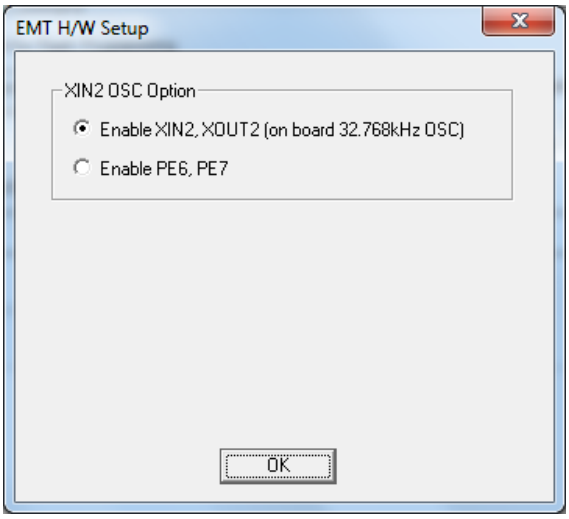
5) ‘Utilities’ Tab - Follow the settings shown below:



6) Click ‘Settings’ in ‘Utilities’ tab to enter Programming Setting. Input relevant settings for programming the emulator chip and then press ‘OK’.



7) Choose either ‘Enable XIN2, XOUT2’ for 32.768kHz oscillator or ‘Enable PE6, PE7’ for I/O usage.



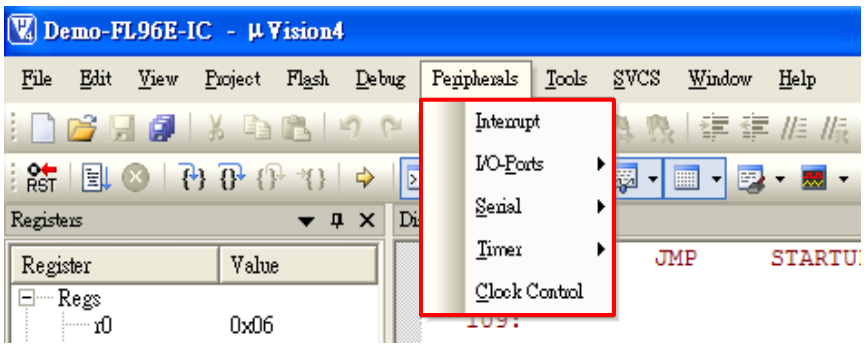
4 View Memory Content

The memory content can be checked in the Keil Memory Windows during debug.

Memory	Size	Memory Type	Start Address	End Address	Example
Program/ Data Flash	Up to 31KB	code	0x00000	0x7BFF	C:0x00000
Internal SRAM	256 bytes	idata	0x00	0xFF	I:0x00
Expanded SRAM	512B	xdata	0x0200	0x03FF	X:0x0200
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

5 Limitations

1) Keil IDE debugger:
   a) DragonICE does not support these peripheral features.



   b) Debug 'Step', 'Step over' will fail if the instruction is entering stop mode while RTC interrupt already enabled before.
2) Keil uVision: uv2 or uv3 cannot be supported by DragonICE. After installing uv4, open and close the project and you will see the option to upgrade the project to uv4 format (*.uvproj).
3) Voltage Supply: The voltage supply to emulator chip is 3.3V (VDD pin voltage). User should do emulation at this voltage level only.
4) MCU Peripherals: When the emulator running is stopped in debugging environment, all the running MCU peripherals (e.g. LCD driver, timer) would still keep running. Thus, the MCU peripherals would be out of synchronization with the code instruction.
5) Compile Keil Project: Only compile the code before entering the Keil debugging environment. Otherwise the emulated flash content may not be updated and the debug action may not match with the displayed code. For example,
   a) Cursor jumped to a wrong code location in debugger.
   b) Debug ‘Step’ wrongly executed as debug ‘Free Run’.
6) SFR/XFR:
   a) CLKC2 bit 6 always turns on XIN in emulator.
   b) CLKC0[2:0] can only write either 001/010/100. Others are invalid.

5.1 Instruction limitation on DC6388EMT-FD

After executing any of instructions (Group A), the next instructions (Group B) reading any non-CPU Special function registers (SFRs) will get 00H.

Group A	Group B
INC dir	ADD A,dir
DEC dir	ADDC A,dir
ANL dir,A	SUBB A,dir
ANL dir,#data	INC dir
ORL dir,A	DEC dir
ORL dir,#data	ANL A,dir
XRL dir,A	ORL A,dir
XRL dir,#data	XRL A,dir
CLR bit	CJNE A,dir,rel
SETB bit	DJNZ dir,rel
CPL bit	MOV A,dir
	MOV Rn,dir
	MOV dir,dir
	MOV @Ri,dir
	PUSH dir
	POP dir
	XCH A,dir

where dir is any non-CPU SFR. Detail refers to section 2 non-CPU SFR.

Example:

Routine	X (Wrong)	Y (Correct)
Group A	ORL dir,#0FFH	ORL dir,#0FFH
		NOP
Group B	MOV PA,dir	MOV PA,dir
Result	Port A output 00	Port A output FF

Solution:
The rule is that group A and B cannot be consecutive.

Therefore, by this rule, software fix can insert NOP between 2 instructions.
C language can use _nop_().

The SFR is classified into two groups:
1) CPU SFRs
2) Non-CPU SFRs
Any SFR registers not in the group ‘CPU SFRs’ will fall into this group.

Table of CPU SFRs

Addr(hex)	Name	Symbol
80	Port A	PA
81	Stack pointer	SP
82	Data Pointer Lo-Byte	DPL
83	Data Pointer Hi-Byte	DPH
84	Data Pointer 1 Lo-Byte	DPL1
85	Data Pointer 1 Hi-Byte	DPH1
86	Data Pointer Select	DPS
87	Power Control	PCON
88	Tmr/Cnt Control	TCON

Addr(hex)	Name	Symbol
89	Tmr/Cnt Mode Control	TMOD
8A	Tmr/Cnt 0 Lo-Byte	TL0
8B	Tmr/Cnt 1 Lo-Byte	TL1
8C	Tmr/Cnt 0 Hi-Byte	TH0
8D	Tmr/Cnt 1 Hi-Byte	TH1
90	Port B	PB
91	Interrupt Request Control Register	IRCON
94	Program Memory Page Selector	PAGESEL
95	External Data Memory Page Selector	D_PAGESEL
98	Serial Control 0 Register	SCON0
99	Serial Data Buffer 0 Register	SBUF0
9A	Interrupt Enable 2	IEN2
A0	Port C	PORTC
A8	Interrupt Enable Register 0	IEN0
AA	Serial 0 Reload Register Lo-byte	S0RELL
B0	Port D	PORTD
B8	Interrupt Priority Register 0	IP0
BA	Serial 0 Reload Register Hi-byte	S0RELH
C0	Port E	PORTE
C8	Timer 2 Control	T2CON
C9	Timer 2 Mode Control	T2MOD
CA	Reload Timer 2 Lo-byte	RCAP2L
CB	Reload Timer 2 Hi-byte	RCAP2H
CC	Tmr/Cnt 2 Lo-Byte	TL2
CD	Tmr/Cnt 2 Hi-Byte	TH2
D0	Program Status Word	PSW
D8	Serial Port 0 Baud Rate Select	ADCON
E0	Accumulator	ACC
E8	Interrupt Enable 1	IEN1
F0	Register B	B
F7	Software Reset	SRST
F8	Interrupt Priority 1	IP1

6 Revision History

The following table shows the revision history for this document.

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	Sep, 2014			First release	Celia Ki	Danny Ho
1.1	Oct, 2014	1.1 1.3 2.2		Add supported products section Add useful links section Add note to IDE Connection section	Celia Ki	Danny Ho
1.2	Jul, 2014	5		Add new items	Danny Ho	Celia Ki
1.3	Nov, 2017	5		Add new item	Danny Ho	Patrick Li

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