DC6688BT96U

Bluetooth BLE Enabled 8051 Flash MCU with IR

DC6688BT96U is a series of 8-bit Microcontroller with Bluetooth Low Energy (BLE) engine embedded for infra-red (IR) IoT application. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, FLASH memory, and peripherals suitable for battery-operated & handheld IR IoT device. The embedded Bluetooth engine is compliant with Bluetooth 4.2 Bluetooth Low Energy system and can handle the bottom 4 layers / protocol autonomously, with a powerful and fully integrated 2.4GHz radio providing a reliable RF solution with the lowest BOM count.

Features

- Bluetooth engine
  - Single-ended RF output. No matching required for typical 0 ~ 3dBm output
  - Maximum radio power: Tx 8dBm, Rx -90dBm
  - Automatic BLE 4.2 stack and security management
    - *GAP role: broadcast, observer, and peripheral with multi-role supported*
    - *GATT server: up to 38 Characteristics with up to 512 bytes for each entry*
    - *SMP: Numeric Comparison, Passkey Entry, Out of Band, or Just Works*
  - 16MHz 7~10pF CLOAD crystal supported
  - Built-in 32kHz RC for automatic periodic transmission
  - Built-in 128KB ROM (patchable) and 4KB SRAM dedicated for BLE 4.2 stack
- High-Performance 1T 8051 8-bit CPU core (1MIPS/MHz), MCS51 instructions compatible
  - 12MHz RC clock generator (±1%) with selectable divider
  - 23 GPIOs: 22 x LED driving capable GPIO + 1 x 300mA IR LED Driver
  - 16-bit Timers x 3, PWM x 3, I^2C, USART x 2, SPI Master
- User Application Memory
  - 95KB Flash memory configurable for code or data memory
  - 256B Internal SRAM + 3KB Extended SRAM
- IR Transceiver
  - IR carrier modulator with built-in high current IR LED driver for IR code transmission
  - IR receive amplifier with 24 bit timer for IR learning capability
- Power Monitor for low battery indicator
  - Low Voltage Detection (LVD)
  - 4 Selectable Low Voltage Indication (LVI) level
- Operating voltage: 2.0 ~ 3.6V
- Current Consumption
  - Advertising (Interval): 0.35mA (200ms), 0.14mA (1s)
  - Keep Connect (Interval): 32uA (1s), 11uA (4s)
  - Deep Sleep: 10uA
  - Remote Control battery lifetime estimate[1]
    - *CR2032 battery: 1.5 Years*
    - *AAA (UM4) x 2 batteries: 8.5 Years*
- Operating temperature: -40°C to +85°C
- Package type:
  - 56 QFN (8x8mm 0.5 pitch)

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Remarks:
[1] User usage calculation: 0.5 hours user input + 23.5 hours idle

Quick look on Ordering Information

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Input RF level	P_{RX}	-	10	dBm
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for all I/O ports[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for all I/O ports[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:
[1] It is measured for any one of I/O pin when configured to push-pull output high.
[2] It is measured as total for all I/O pots when configured to push-pull output high.
[3] It is measured for any one of I/O pin when configured to push-pull output low.
[4] It is measured as total for all I/O pots when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz/16MHz	2.0	-	3.6	V
Input High Voltage	V_{IH1}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input pins	0	-	0.3 V_{DD}	V
Output High Voltage	V_{OH1}	Port C1, V_{DD} = 2.4V, I_{OH} = - 6mA, T_A = 25°C	V_{DD} – 0.7	-	-	V
	V_{OH3}	Other port except Port C1, V_{DD} = 2.4V, I_{OH} = -2.2mA, T_A = 25°C	V_{DD} – 0.7	-	-	V
Output Low Voltage	V_{OL1}	Port C1, V_{DD} = 2.4V, I_{OL} = 12mA, IRDRV disabled, T_A = 25°C	-	0.4	1	V
	V_{OL3}	All output pins except Port C1, V_{DD} = 2.4V, I_{OL} = 12mA, T_A = 25°C	-	0.4	1	V
Output Low Current IR Transmit	$I_{OL(IRTX)}$	V_{OL} = 0.5V, IRDRV = 3, T_A = 25°C	-	300	-	mA
Input High Leakage Current	I_{LIH1}	All input pins except PROG, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH3}	PROG, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins, V_{IN} = 0	-	-	-1	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	40	80	160	kΩ
Pull-down Resistors	R_{PD}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current Run Mode [1]	Idd(op)	f_{OSC} = 12MHz/16MHz, V_{DD} = 3.0V, T_A = 25°C	-	2	8	mA
Supply Current Power Down Mode [2]	Idd(pd)	V_{DD} = 3.0V, Bit 7(T24_CON1) = 0, T_A = 25°C	-	7	10	μA

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull and radio turned off.

[2] Supply current is tested if the condition is that:

a) Port A output open-drain.

b) Port B and C input enable pull-up resistor.

c) Port C1 output push-pull.

d) Port D output push-pull.

1.3 Radio Characteristics

(T_A = -25-70°C)

Parameter	Conditions	Min	Typ	Max	Unit
Operation Range		2400	-	2483	MHz
Frequency deviation		225	250	275	kHz
On air data rate		-	1M	-	bps
RF channel spacing		-	2	-	MHz
Radio peak current consumption	TX mode: <-40dBm	-	15	-	mA
	TX mode: 2dBm	-	28	-	mA
	TX mode: 8dBm	-	48	-	mA
	RX mode	-	28	-	mA

1.4 RF Receive

(T_A = 25°C, f_c = 2440MHz)

Parameter	Conditions	Min	Typ	Max	Unit
Receiver sensitivity	Ideal	-	-92	-	dBm
	Dirty	-	-90	-	dBm
Saturation		-	2	-	dBm
Co-channel rejection[4]		-	7	-	dB
Adjacent channel selectivity	±1 MHz offset	-	1	-	dB
	±2 MHz offset	-	-28	-	dB
	±(3+n) MHz offset [n= 0,1,2…]	-	-38	-	dB
Image frequency rejection	As define in Bluetooth V4.2	-	-21	-	dB
	f = f_{RX}+ 4 MHz	-	-23	-	dB
Intermodulation	Minimum interferer level	-	-38	-	dBm

1.5 RF Transmit

(T_A = 25°C, f_c = 2440MHz)

Parameter	Conditions	Min	Typ	Max	Unit
Output power	Delivered to a single-ended 50-Ω load using maximum output power setting	-	8	-	dBm
	Delivered to a single-ended 50-Ω load using minimum output power setting	-	-40	-	dBm
Programmable output power range	Delivered to a single-ended 50-Ω load using minimum output power setting	-	30	-	dB
Optimum load	Impedance as seen from the RF port towards	-	50	-	Ω

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Parameter	Conditions	Min	Typ	Max	Unit
impedance	the antenna				

1.6 16MHz Crystal Oscillator for Radio

(T_A = 25°C)

Parameter	Conditions	Min	Typ	Max	Unit
Crystal frequency		-	16	-	MHz
Crystal frequency accuracy requirement[1]		-	-	±40	ppm
Crystal load capacitance		7	9	10	pF
Start-up time		-	200	-	us

Remarks:
[1] Including aging and temperature dependency

1.7 32-kHz RC Oscillator for periodic RF transmission

(T_A = 25°C)

Parameter	Conditions	Min	Typ	Max	Unit
Calibrated frequency		-	32768	-	Hz
Frequency accuracy	After auto calibration	-	-	±250	ppm
Start-up time		-	200	-	us

1.8 RSSI Characteristics

(T_A = 25°C)

Parameter	Conditions	Min	Typ	Max	Unit
RSSI range[1]		-	45	-	dB
RSSI minmum level[1]		-	-83	-	dBm
RSSI accuracy[1]		-	-	±5	dB
Step size (LSB value)		-	0.4	-	dB

Remarks:
[1] Assuming DC6688BT96U reference design.

1.9 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Program setting	1.65	1.8	1.95	V
		Default setting	2.0	2.15	2.3	V
		Program setting	2.35	2.5	2.65	V
		Program setting	2.65	2.8	2.95	V
Low Voltage Detect Level	V_{LVD1}		1.4	1.5	1.6	V

Remarks:
[1] $V_{LVD2} - V_{LVD1} = \Delta V$

1.10 SRAM Data Retention Voltage

(T_A = -40°C to +85°C)

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Current	I_{DDDR}	V_{DDDR} = 1.0V, Stop mode	-	-	1	uA

1.11 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.12 Flash Memory Data Retention

(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.13 Internal System RC Oscillation Characteristics

Oscillator	Conditions	Min	Typ	Max	Unit
Internal system RC Oscillator Accuracy	T_A = -20°C to +70°C, V_{DD} = 1.8V to 3.6V	-	-	± 1%	MHz
Internal 50kHz Oscillator	T_A = -20°C to +70°C	-	50	-	kHz

(T_A = -40°C to +85°C, V_{DD} = 3.0V)

Parameter	Conditions	Min	Typ	Max	Unit
Oscillator Stabilization Wait Time	t_{WAIT} when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
	t_{WAIT} when released by an external interrupt[2]	-	$2^{13}/f_{OSC}$	-	ms

Remarks:
[1] f_{osc} is the oscillator frequency.
[2] The duration of the oscillation stabilization time(t_{WAIT}) when it is released from power down mode by PA or PB interrupt.

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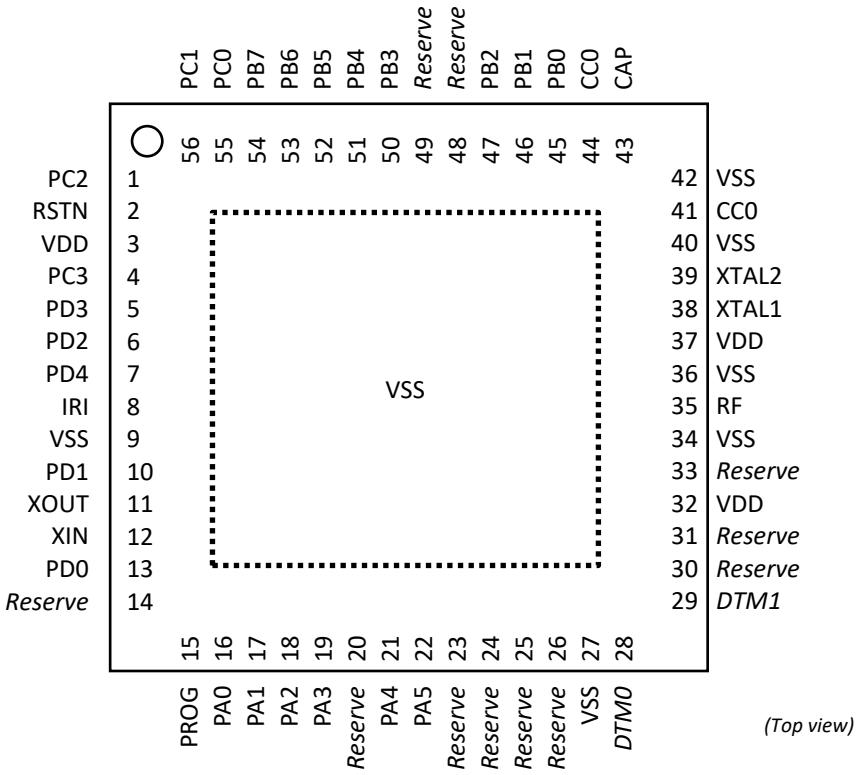
2 Pin Assignment

(QFN56)



(Top view)

Power

Pin	Function	Decoupling
VDD	VDD supply	220uF (Shared) + 100nF
CAP	Voltage reference	1uF
VSS	MCU & Radio Power Ground	-

GPIO

Pin	GPIO Function	USART	I2C0	I2C1	SPI	Timer	PWM	IR	ISP
PA0	Interruptible; Type A	-	-	-	-	-	-	-	-
PA1	Interruptible; Type A	-	-	-	-	-	-	-	-
PA2	Interruptible; Type A	-	-	-	-	-	-	-	-
PA3	Interruptible; Type A	-	-	-	-	-	-	-	-
PA4	Interruptible; Type A	-	-	-	-	-	-	-	-
PA5	Interruptible; Type A	-	-	-	-	-	-	-	-
PB0	Interruptible; Type A	RX0	-	-	-	-	-	-	-
PB1	Interruptible; Type A	TX0	-	-	-	-	-	-	-
PB2	Interruptible; Type A	RX1	-	-	SDI	-	-	-	-
PB3	Interruptible; Type A	TX1	-	-	SDO	-	-	-	-
PB4	Interruptible; Type A	-	-	SCL1	SCK	-	-	-	-
PB5	Interruptible; Type A	-	-	SDA1	-	-	PWM0	-	-
PB6	Interruptible; Type A	-	-	-	-	T2EX/ T24EX	PWM1	-	ECLK2
PB7	Interruptible; Type A	-	SDA0	-	-		-	-	-

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PC0	Interruptible; Type A	-	SCL0	-	-	T0	-	-	-
PC1	Interruptible; Type A	-	-	-	-	T1/T24	-	REM/ IRTx	-
PC2	Interruptible; Type A	-	-	-	-	T2/ T24CLK	-	-	-
PC3	Interruptible; Type A	-	-	-	-	-	-	-	-
PD0	Type B	-	-	-	-	-	-	-	SL
PD1	Type B	-	-	-	-	-	-	-	ECLK
PD2	Type B	-	-	-	-	-	-	-	-
PD3	Type B	-	-	-	-	-	-	-	-
PD4	Type B	-	-	-	-	-	-	-	-

GPIO Type A: Hi-Z, or Totem Pole, or N-ch OD; Each mode w/ selectable pull-up/pull-down resistor
GPIO Type B: Hi-Z w/ selectable pull-up/pull-down resistor, or Totem Pole, or N-ch OD

Special

Pin	Function
RSTN	Reset (Active Low) signal input
IRI	IR receive amplifier (IR LED) input
DTM0, DTM1	DTM UART interface required by Bluetooth 4.2
CC0	Close Connection Pin. Connect the pins pair externally via PCB.
PROG	In-System Programming selection input
XIN, XOUT	Optional external MCU Crystal connection
XTAL1, XTAL2	Radio Crystal connections (default: 16MHz, 9pF loading) (Order selectable: 12, 24, 26, 32, 40MHz; 10pF loading)
RF	Single-ended Radio Antenna connection

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3 Overview

DC6688BT96U MCU series consists of an excellent performance autonomously BLE engine, a proven Infra-Red Transceiver, a 1MIPS/MHz high performance 8051 MCU, and TSMC's in-system/on-field programmable Flash memory.

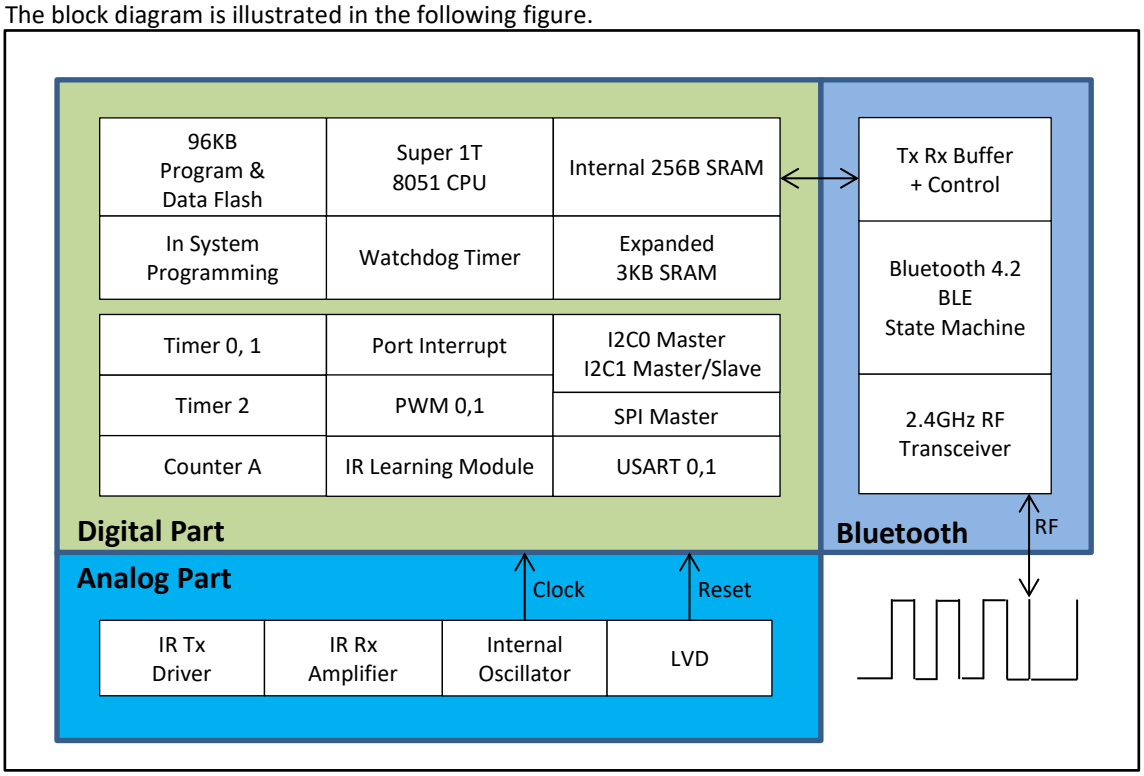
The embedded Bluetooth BLE engine conforms to Bluetooth Low Energy specification 4.2. The radio supports single-end RF output of up to 8dBm, with automation of broadcast, observer, and peripheral GAP roles.

With the 1T 8051 8-bit CPU as application processor, instruction execution time is just 83.3ns at 12Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

The low voltage operated Flash memory block is designed and embedded for both program and data memory. In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. In addition, the Flash memory can also be re-programmed by user program, with protection mechanism to avoid accidental re-programming, for storing data or the on-the-field updates.

Internal RC oscillator for application CPU is equipped and operated at 16MHz, 12MHz, 8MHz, 6MHz, 4MHz, 2MHz and 1MHz software selectable without external components. It supports trimming by In-System Programmer to ensure the oscillator within specification.

The block diagram is illustrated in the following figure.



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4 Bluetooth Low Energy Engine

DC6688BT96U incorporated a Bluetooth low energy (BLE) engine which is compliant with Bluetooth low energy specification 4.2. The engine consists of a 2.4 GHz radio transceiver, modem, and state machine, allows the engine to advertise, scan and maintain connections autonomously with minimal user software input.

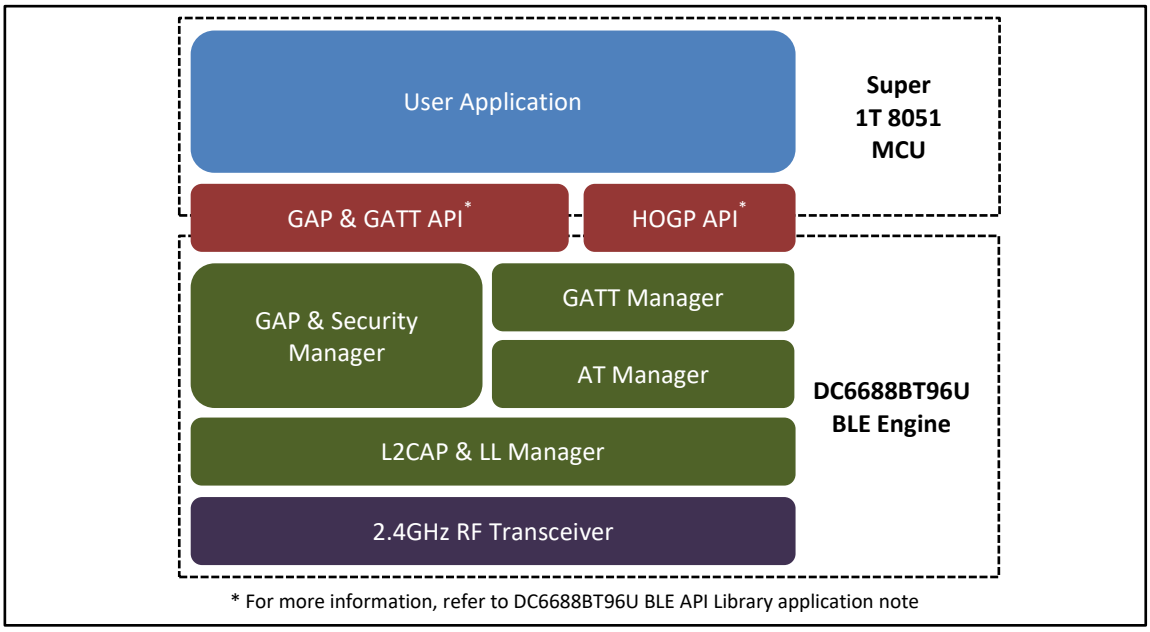
The DC6688BT96U uses a fully integrated 2.4 GHz radio transceiver, with its single-ended 50 ohm impedance matched, and with output power up to 8 dBm. This allows using antenna without matching for typical application for power up to 3 dBm thus minimizing the application BOM count, or long-range application without additional component and complicated antenna design.

The BLE engine integrated the Link Layer and Host Controller Interface logic with integrated BLE security support. The engine supports broadcaster, observer, and peripheral GAP roles, and up to 38 GATT characteristics, of which up to 512 bytes of data per characteristic. Security primitives are provided to manage the Link Layer Security for Security Manager / Out of Band pairing and encryption flow.

A single 16MHz crystal is used for frequency reference for the radio and self-calibrating RC timer. The RC timer enables the engine to advertise and maintain connections in interval from 7.5ms to 10 seconds automatically. The engine supports 16MHz crystal with capacitor loading between 7 ~ 10pF of tolerance up to 40 ppm.

Since the BLE engine handles the entire low-level communication layer automatically, application only requires populating the BLE data and access routines. As part of the standard, we provide a programming library, Dragonchip BLE Library, to standardize the setup and access handler process in conformance to the BLE guidelines. The DC BLE Library supports GAP, GATT, ANCS, HOGP…etc with example code available. Please refer to the BLE Library documentation for more details.

DC6688BT96U BLE Architecture



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5 Memory

Memory comprises of the following elements, namely:

- 95KB Program Flash memory + Data Flash memory
- 256B Internal SRAM
- 3KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

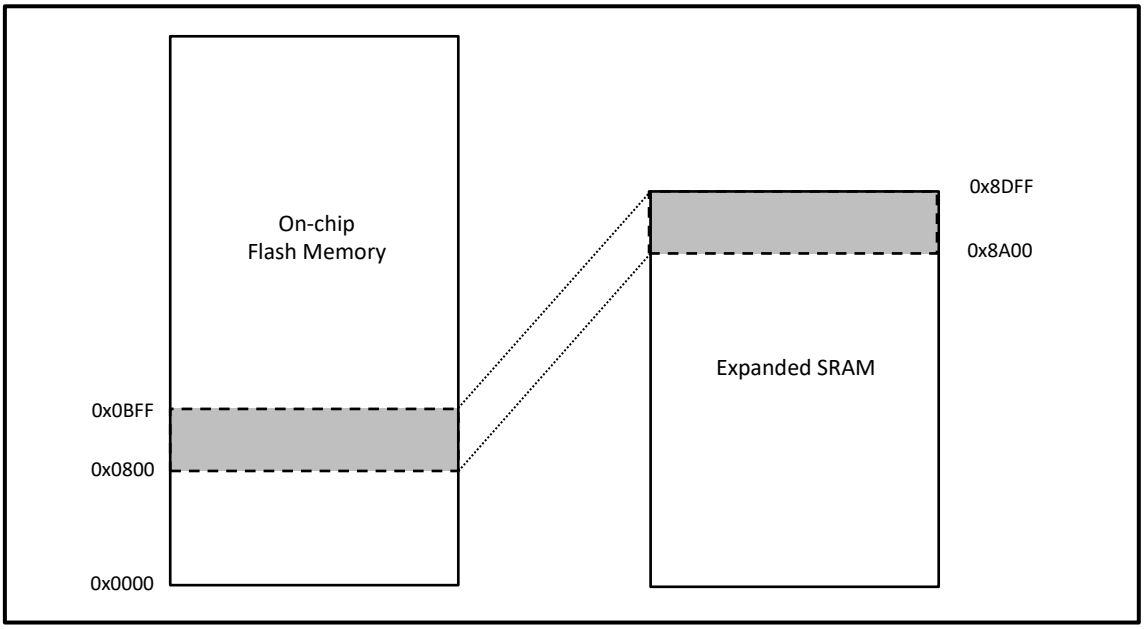
5.1 Program & Data Flash Memory

The built-in Flash memory can be programed via In-System Progamming(ISP) system, where it can be partitioned in 512 byte block from 2.5KB bytes to be used as program memory while the remaining area as data memory.

User program can write data to the data partition of the Flash memory via the embedded expand SRAM, with the write protection signature option to avoid writing accidentally.

5.2 Code Executable from SRAM

Code execution enables the mapping of Flash memory to SRAM. This SRAM segment replaces the on-chip Flash memory.



5.3 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, USART, etc. Some locations in the SFR address space are addressable as bits.

5.4 External Function Register (XFR)

The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

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6 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

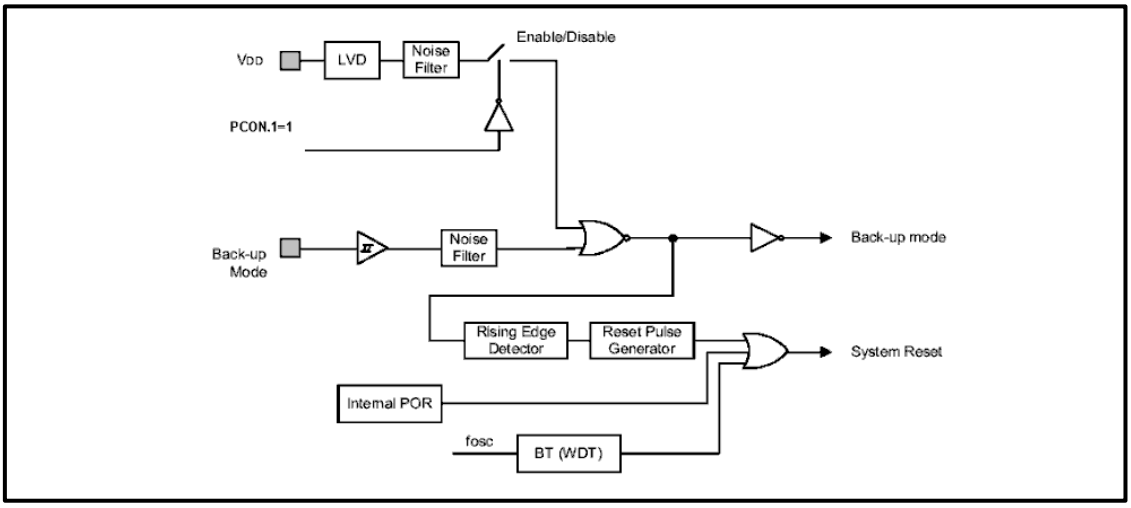
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

7 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



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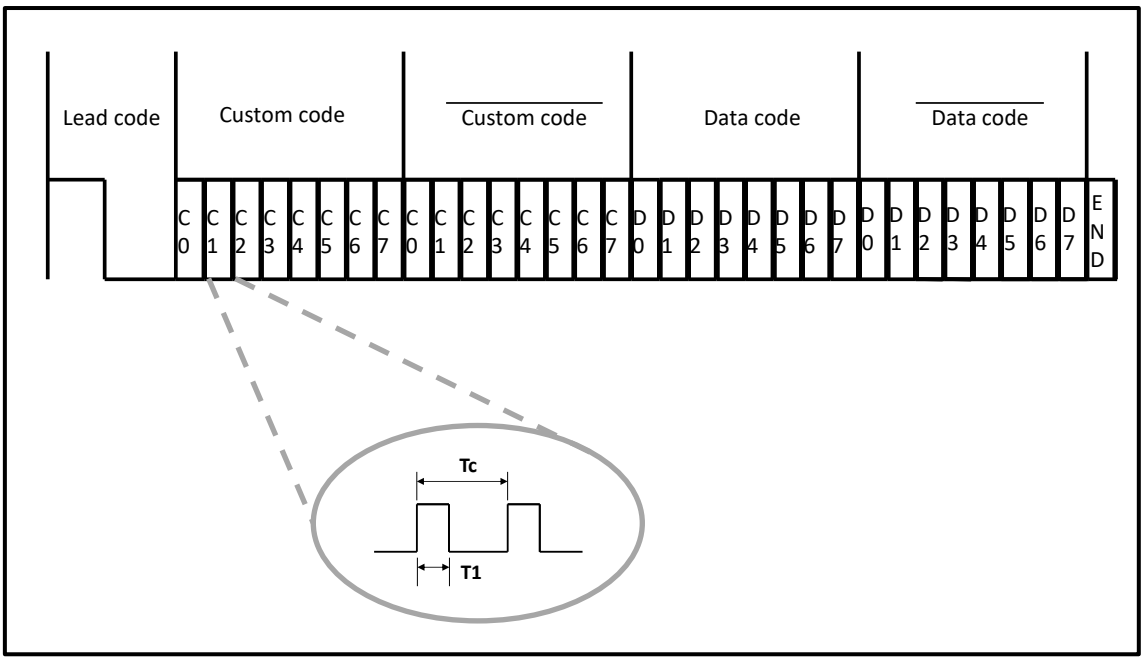
8 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

9 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator

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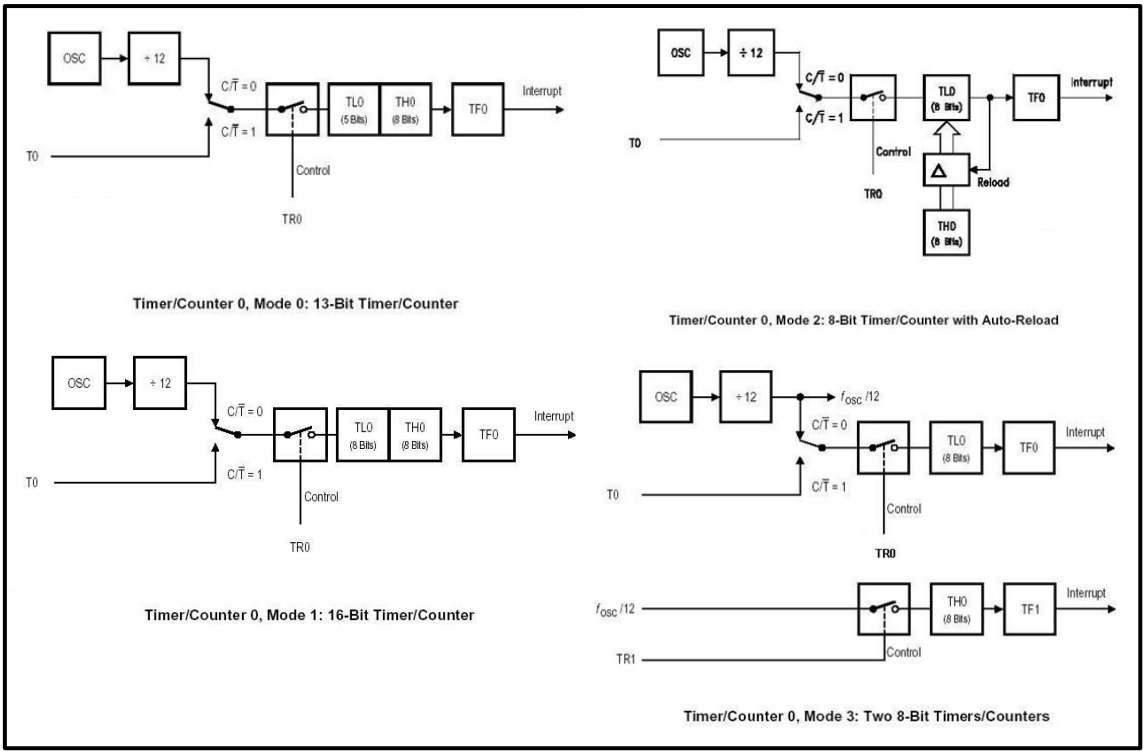

10 Enhanced USART

The enhanced USART peripheral support both asynchronous and synchronous mode with dedicated clock divider to generate common baud rate with minimal offset. It has a transmission and reception buffer with interrupt allows for full duplex USART communication. It also support multi-node communication via 9 bit USART mode.

11 Serial Peripheral Interface

A complete hardware Serial Peripheral Interface (SPI) on-chip in master mode is integrated. SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously.

The SPI interface consists of the following wires:

- SDI
  The SDI line on the master (data in) should be connected to the SDO/MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.
- SDO
  The SDO line on the master (data out) should be connected to the SDI/MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.
- SCK
  The master serial clock (SCK) is used to synchronize the data being transmitted and received through the SDO and SDI data lines. A single data bit is transmitted and received in each SCK period. Therefore, a byte is transmitted/received after eight SCK periods.
- SS
  In the slave device, SPI interface requires the slave select line (SS) to enable communication such that DC6688FLT (master) can talk to more than one slave device in different time slot. To be able to talk to the slave device, master should assert the SS pin on an external slave device. This can be done by using a Port digital output pin which is manually controlled by software.

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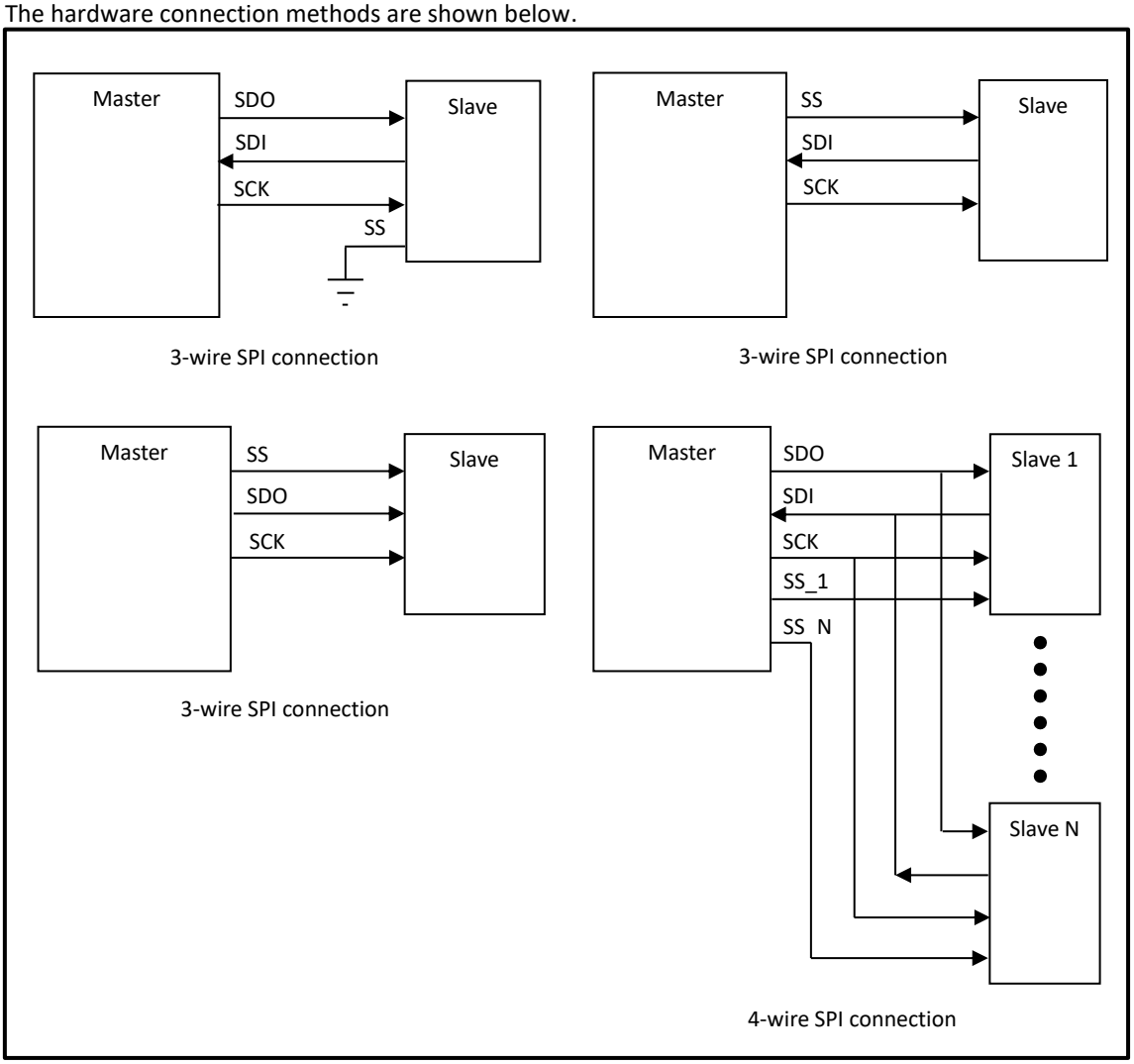
The hardware connection methods are shown below.



12 Inter-Integrated Circuit (I2C) Interface

The I2C Bus Controller supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: “SCL” (serial clock line) and “SDA” (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus.

The interface defines 2 transmission speeds if 12MHz crystal is used:
- Normal: 100Kbps
- Fast: 400Kbps

The I2C component performs 8-bit-oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode and may operate in the two modes.

Mode	Description
Master Transmitter Mode	Serial data output through SDA while SCL output the serial clock.
Master Receiver Mode	Serial data is received via SDA while SCL outputs the serial clock.
Slave Receiver Mode	Serial data and the serial clock and received through SDA and SCL
Slave Transmitter Mode	Serial data is transmitted via SDA while the serial clock is input through SCL

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13 Infrared Learning Module

IR learning module includes IR receiver and T24 timer. Analog signal entering IRI pin is converted to digital signal by IR receiver, and feed to T24 timer.

With the built-in Op Amp circuit, no external amplifier circuit is needed. The high resolution 24-bit timer provides a high capability of IR learning. It can capture carrier frequency as high as 500kHz.

14 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires 6 wires to minimize the number of added components and board area impact.

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15 Ordering Information

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688BT96UZ	QFN56	96KB Configurable		256B + 3KB	23
DC6688BT96UZ-TR1[1]	QFN56	96KB Configurable		256B + 3KB	23

[1] Tape and reel packing.

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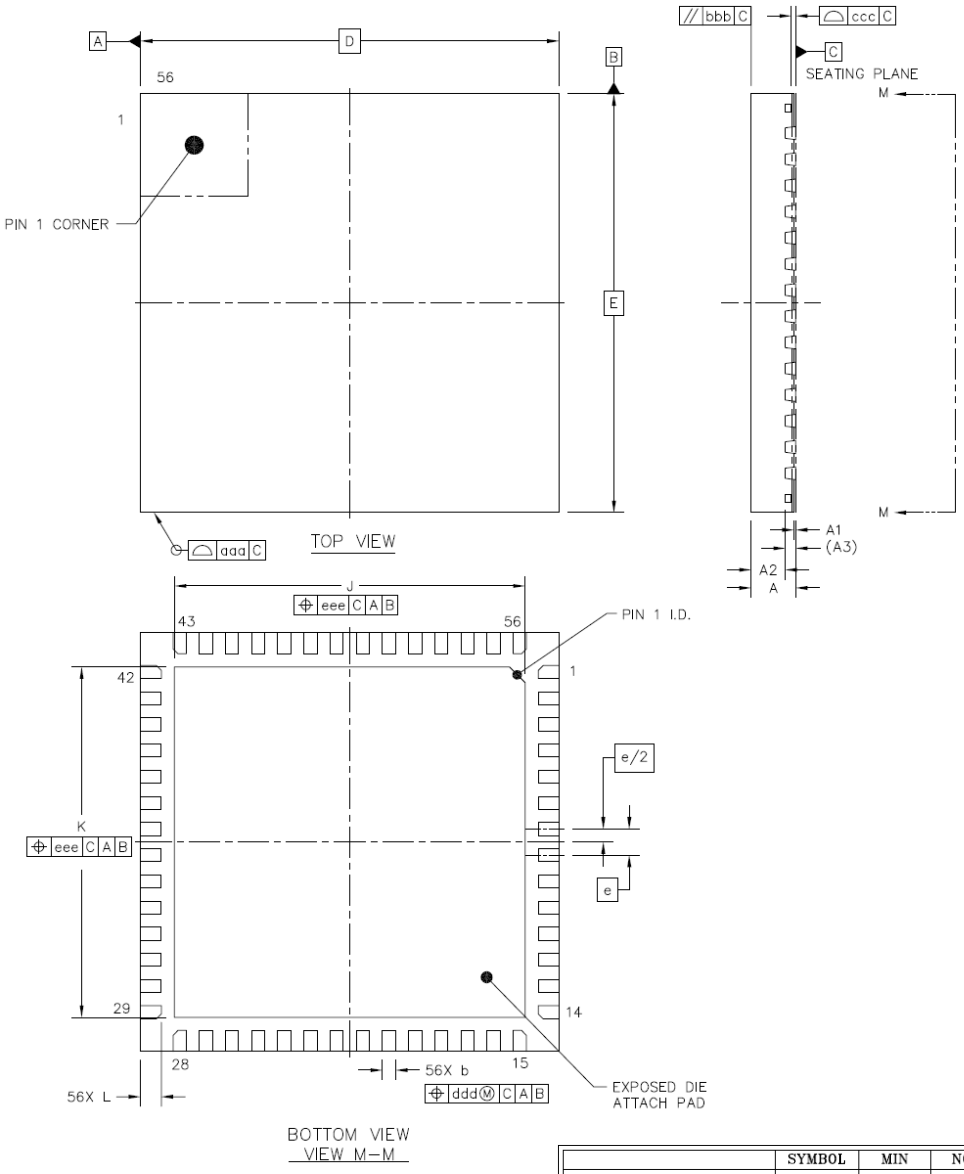
16 Package Outlines

16.1 56-pin QFN



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	6.6	6.7	6.8
	Y	K	6.6	6.7	6.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

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17 Revision History

Document Rev No.	Issued Date	Section	Description	Edited by	Reviewed by
1.0	2017	All	Initial Release	Kennis To	Patrick Li
1.1	Nov, 2017	2	Revise pin assignment	Kennis To	Patrick Li
1.2	Dec, 2017	Front page	Add feature	Kennis To	Patrick Chan
1.3	Feb 2018	All	Revise pin assignment; Change from BT96T to BT96U	Patrick Chan	Danny Ho
1.4	Jan 2019	2,3	Removed Port D interruptible Added I2C0 (master-only) to PB7 & PC0	Patrick Chan	Patrick Li

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