



DC6688F2SEN

Single Battery Operated Microcontroller

DC6688F2SEN is a 8-bit Micro Controller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with turbo mode 80C51 CPU core, Flash program memory, peripherals suitable for battery-operated applications, LCD Monitor, Home Appliance and A/V equipment. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and more importantly, inventory burden.

Features

- ◆ Enhanced 8051 8-bit CPU core, MCS51 instructions compatible
- ◆ Power Down and Backup modes
- ◆ Single battery operated (1.2V-1.8V)
- ◆ Memory
 - ◇ 2KB Configurable Program & Data Flash Memory
 - ◇ Security bit for read back protection
 - ◇ 64B SRAM
- ◆ IR generator by counter A with auto-reload function
- ◆ Built-in transistor for IR LED ($I_{OL} = 100\text{mA}$ at $V_{OL} = 0.25\text{V}$)
- ◆ Two-level priority interrupt controller
- ◆ 16 bit-programmable I/O ports
- ◆ 16-bit Timers x 3
- ◆ Low Voltage Detection (LVD) for backup mode
- ◆ Maximum operating voltage: 1.8V
- ◆ Operating temperature: -40°C to $+85^{\circ}\text{C}$
- ◆ Package type:
 - ◇ 20-pin TSSOP
 - ◇ 20-pin SSOP
 - ◇ 16-pin SOP

Quick look on [Ordering Information](#)

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

($T_A = 25^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Conditions | Rating | Unit |
|-----------------------|-----------|---|------------------------|------------------|
| Supply Voltage | V_{DD} | - | -0.3 to +3.8 | V |
| Input Voltage | V_{IN} | - | -0.3 to $V_{DD} + 0.3$ | V |
| Output Current High | I_{OH} | One I/O pin active[1] | -18 | mA |
| | | Total pin current for ports A,B and C[2] | -60 | mA |
| Output Current Low | I_{OL} | One I/O pin active[3] | +30 | mA |
| | | Total pin current for ports A,B and C[4][5] | +100 | mA |
| Operating Temperature | T_A | - | -40 to +85 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | - | -65 to +150 | $^\circ\text{C}$ |

Remarks:

- [1] It is measured for any one of I/O pin when configured to push-pull output high.
 [2] It is measured as total for Ports A, B and C when configured to push-pull output high.
 [3] It is measured for any one of I/O pin when configured to push-pull output low.
 [4] It is measured as total for Ports A, B and C when configured to push-pull output low.
 [5] Exclude Port C1 when IR driver is active

1.2 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

| Parameter | Symbol | Value | Unit |
|--------------------------------------|-------------|-------|------|
| ESD Target for Machine Model (MM) | V_{THMM} | 200 | V |
| ESD Target for Human Body Model (MM) | V_{THHBM} | 2000 | V |

1.3 DC Electrical Characteristics

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD} = V_{LVD1}$ to 1.8 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------|--|----------------|-----|--------------|------|
| Operating Voltage | V_{DD} | $f_{OSC} = 12\text{MHz}$ | V_{LVD1} | - | 1.8 | V |
| Input High Voltage | V_{IH1} | All input pins except XIN | $0.7 V_{DD}$ | - | V_{DD} | V |
| | V_{IH2} | XIN | $V_{DD} - 0.3$ | - | V_{DD} | V |
| Input Low Voltage | V_{IL1} | All input pins except XIN | 0 | - | $0.3 V_{DD}$ | V |
| | V_{IL2} | XIN | 0 | - | 0.3 | V |
| Output High Voltage | V_{OH1} | Port C1, $V_{DD} = 1.3\text{V}$, $I_{OH} = -3\text{mA}$, $T_A = 25^\circ\text{C}$ | $V_{DD} - 0.4$ | - | - | V |
| | V_{OH2} | Port C0, C2, $V_{DD} = 1.3\text{V}$, $I_{OH} = -1.1\text{mA}$, $T_A = 25^\circ\text{C}$ | $V_{DD} - 0.4$ | - | - | V |
| | V_{OH3} | All output pins except Port C pins, $V_{DD} = 1.3\text{V}$, $I_{OH} = -0.5\text{mA}$, $T_A = 25^\circ\text{C}$ | $V_{DD} - 0.5$ | - | - | V |
| Output Low Voltage | V_{OL1} | Port C1, $V_{DD} = 1.3\text{V}$, $I_{OL} = 6\text{mA}$, $T_A = 25^\circ\text{C}$ | - | 0.3 | 0.6 | V |
| | V_{OL2} | Port C0, C2, $V_{DD} = 1.3\text{V}$, $I_{OL} = 6\text{mA}$, T_A | - | 0.3 | 0.6 | V |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|-----------------------|--|-----|-----|-----|------|
| | | = 25°C | | | | |
| | V _{OL3} | All output pins except Port C pins, V _{DD} = 1.3V, I _{OL} = 0.5mA, T _A = 25°C | - | 0.3 | 0.6 | V |
| Output Low Current IR Transmit | I _{OL(IRTX)} | V _{OL} = 0.25V, IRDRV = 3, T _A = 25°C | - | 100 | - | mA |
| High Level Output Current REM | I _{OH(peak)} | V _{DD} = 1.5V, peak value | - | - | -10 | mA |
| | I _{OH(avg)} | V _{DD} = 1.5V, average value | - | - | -5 | mA |
| Low Level Output Current REM | I _{OL(peak)} | V _{DD} = 1.5V, peak value | - | - | 2 | mA |
| | I _{OL(avg)} | V _{DD} = 1.5V, average value | - | - | 1 | mA |
| Input High Leakage Current | I _{LIH1} | All input pins except XIN, XOUT and ISPSEL, V _{IN} = V _{DD} | - | - | 1 | μA |
| | I _{LIH2} | XIN and XOUT, V _{IN} = V _{DD} | - | - | 20 | μA |
| | I _{LIH3} | ISPSEL, V _{IN} = V _{DD} | - | - | 100 | μA |
| Input Low Leakage Current | I _{LIL1} | All input pins except XIN and XOUT, V _{IN} = 0 | - | - | -1 | μA |
| | I _{LIL2} | XIN and XOUT, V _{IN} = 0 | - | - | -20 | μA |
| Output High Leakage Current | I _{LOH} | All output pins, V _{OUT} = V _{DD} | - | - | 1 | μA |
| Output Low Leakage Current | I _{LOL} | All output pins, V _{OUT} = 0V | - | - | -1 | μA |
| Pull-up Resistors | R _{PU} | V _{DD} = 1.5V, V _{IN} = 0 V; T _A = 25°C | 75 | 150 | 300 | kΩ |
| Supply Current Run Mode[1] | I _{dd(op)} | f _{OSC} = 4MHz, V _{DD} = 1.5V, T _A = 25°C | - | 1 | 1.5 | mA |
| Supply Current Power Down Mode[2] | I _{dd(pd)} | V _{DD} = 1.5V, T _A = 25°C | - | 1 | 1.5 | μA |

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is tested if the condition is that:

- a) Port A output open-drain.
- b) Port B and C0, C2 input enable pull-up resistor.
- c) Port C1 output push-pull.

1.4 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-------------------|-----------------------|-----|------|-----|------|
| Hysteresis Voltage of LVD (slew rate of LVD) | ΔV[1] | | - | 100 | - | mV |
| Low Voltage Detect Level | V _{LVD1} | T _A = 25°C | 1.1 | 1.15 | 1.2 | V |

Remarks:

[1] V_{LVD2} - V_{LVD1} = ΔV

1.5 SRAM Data Retention Voltage in Power Down Mode

(T_A = -40°C to +85°C)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|-------------------|------------------------------------|-----|-----|-----|------|
| Data Retention Supply Voltage | V _{DDDR} | | 1.0 | - | 1.8 | V |
| Data Retention Supply Current | I _{DDDR} | V _{DDDR} = 1.0V Stop Mode | - | - | 1 | uA |

1.6 Input/Output Capacitance

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 0\text{ V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|-----------|---|-----|-----|-----|------|
| Input Capacitance | C_{IN} | f = 1MHz; unmeasured pins are connected to V_{SS} | - | - | 10 | pF |
| Output Capacitance | C_{OUT} | | | | | |
| I/O Capacitance | C_{IO} | | | | | |

1.7 Flash Memory Data Retention

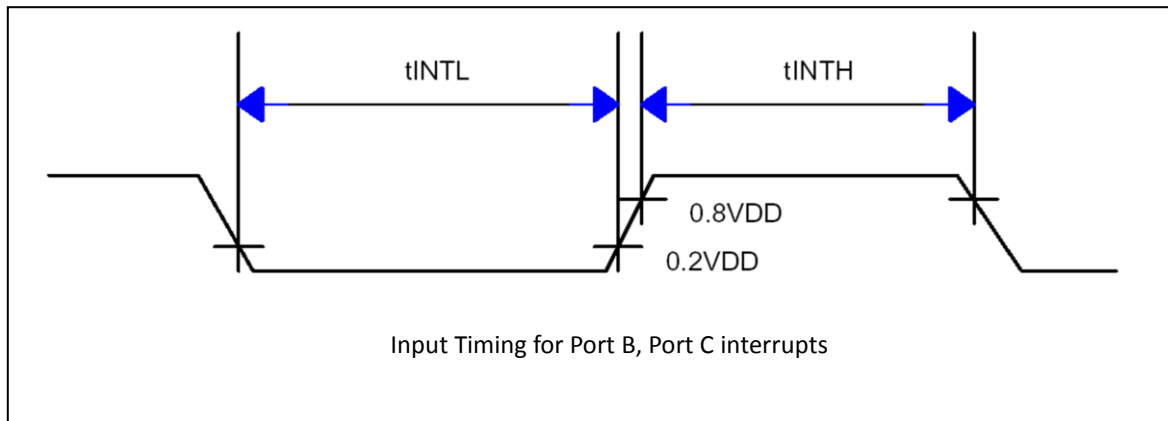
($V_{DD} = 1.5\text{V}$, $T_A = 25^{\circ}\text{C}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------|------------|------------------------|-----|-----|-----|------|
| Data Retention | t_{DRP1} | 1 write/erase cycle | - | 100 | - | Year |
| | t_{DRP2} | 10k write/erase cycle | - | 10 | - | Year |
| | t_{DRP3} | 100k write/erase cycle | - | 1 | - | Year |

1.8 A.C. Electrical Characteristics

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|----------------------------|--|-----|-----|-----|------|
| Interrupt Input High, Low width for Port A | t_{INTH} , t_{INTL} | PB0 – PB3, PB7, PC0, PC2, $V_{DD} = 1.5\text{V}$ | 0 | - | - | - |



1.9 Oscillation Characteristics

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

| Oscillator | Clock Circuit | Conditions | Min | Typ | Max | Unit |
|----------------|---------------|---------------------------------|-----|-----|-----|------|
| Crystal | | CPU clock oscillation frequency | 1 | - | 4 | MHz |
| Ceramic | | CPU clock oscillation frequency | 1 | - | 4 | MHz |
| External Clock | | X_{IN} input frequency | 1 | - | 4 | MHz |

(T_A = -40°C to +85°C, V_{DD} = 1.5V)

| Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--|-----|-----------------------------------|-----|------|
| Crystal | f _{OSC} > 1MHz | - | - | 20 | ms |
| Ceramic | Oscillation stabilization occurs when V _{DD} is equal to the minimum oscillator voltage range | - | - | 10 | ms |
| External Clock | X _{IN} input High and Low width(t _{XL} , t _{XH}) | 25 | - | 500 | ns |
| Oscillator Stabilization Wait Time | t _{WAIT} when released by internal reset[1] | - | 2 ¹² /f _{OSC} | - | ms |
| | t _{WAIT} when released by an external interrupt[2] | - | 2 ¹² /f _{OSC} | - | ms |

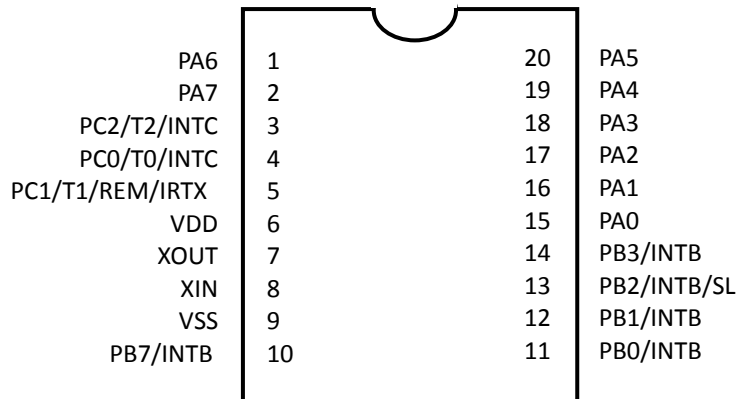
Remarks:

[1] f_{osc} is the oscillator frequency.

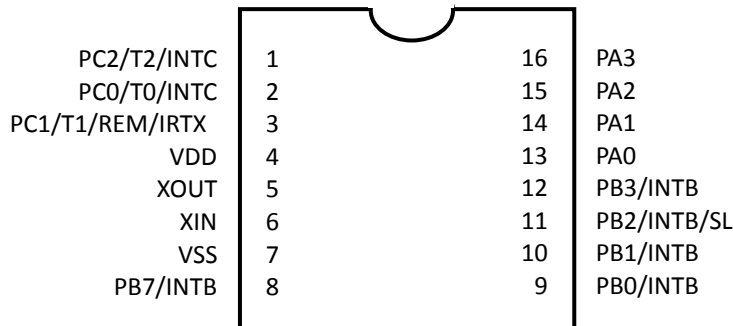
[2] The duration of the oscillation stabilization time(t_{WAIT}) when it is released from power down mode by Port B/Port C interrupt.

2 Pin Assignment

(TSSOP20/SSOP20)



(SOP16)



| TSSOP20 SSOP20 | SOP16 | Pin Name | Symbol | Function |
|-------------------|-------|-------------|--------|---------------------------------------|
| 7 | 5 | XOUT | XOUT | Crystal / oscillator output |
| 8 | 6 | XIN | XIN | Crystal / oscillator input |
| 6 | 4 | VDD | VDD | Power |
| 9 | 7 | VSS | VSS | Ground |
| 15 | 13 | PA0 | PA0 | Configurable input or output port |
| 16 | 14 | PA1 | PA1 | Configurable input or output port |
| 17 | 15 | PA2 | PA2 | Configurable input or output port |
| 18 | 16 | PA3 | PA3 | Configurable input or output port |
| 19 | - | PA4 | PA4 | Configurable input or output port |
| 20 | - | PA5 | PA5 | Configurable input or output port |
| 1 | - | PA6 | PA6 | Configurable input or output port |
| 2 | - | PA7 | PA7 | Configurable input or output port |
| 11 | 9 | PB0/INTB | PB0 | Configurable input or output port |
| | | | INTB | Port interrupt input |
| 12 | 10 | PB1/INTB | PB1 | Configurable input or output port |
| | | | INTB | Port interrupt input |
| 13 | 11 | PB2/INTB/SL | PB2 | Input port |
| | | | INTB | Port interrupt input |
| | | | SL | SL (Single Line) communication signal |
| 14 | 12 | PB3/INTB | PB3 | Configurable input or output port |
| | | | INTB | Port interrupt input |
| 10 | 8 | PB7/INTB | PB7 | Configurable input or output port |
| | | | INTB | Port interrupt input |
| 4 | 2 | PC0/T0/INTC | PC0 | High current drive configurable I/O |
| | | | T0 | Timer 0 external counter input |
| | | | INTC | Port interrupt input |
| 5 | 3 | PC1/T1/REM | PC1 | High current drive configurable I/O |
| | | | T1 | Timer 1 external counter input |
| | | | REM | Counter A carrier frequency output |
| | | | IRTX | IR transmit with built-in transistor |
| 3 | 1 | PC2/T2/INTC | PC2 | High current drive configurable I/O |
| | | | T2 | Timer 2 external counter input |
| | | | INTC | Port interrupt input |

3 Description

DC6688F2SEN is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with 8051 CPU core, Flash memory, and peripherals suitable for battery-operated, LCD Monitor, Home Appliance and A/V equipment. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) and built-in transistor for IR remote controller application. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

4 Memory

Memory comprises of the following elements, namely:

- ◆ 2KB Program Flash memory + Data Flash memory
- ◆ 64B Internal SRAM
- ◆ 128B Special function register (SFR)
- ◆ 256B External special function register (XFR)

4.1 Program & Data Flash Memory

A 2K bytes on-chip program Flash is provided for simple application. It can be programmed by In-System-Programming (ISP) method.

In addition, write protection signature is available to avoid writing accidentally.

4.2 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, etc. Some locations in the SFR address space are addressable as bits.

4.3 External Function Register (XFR)

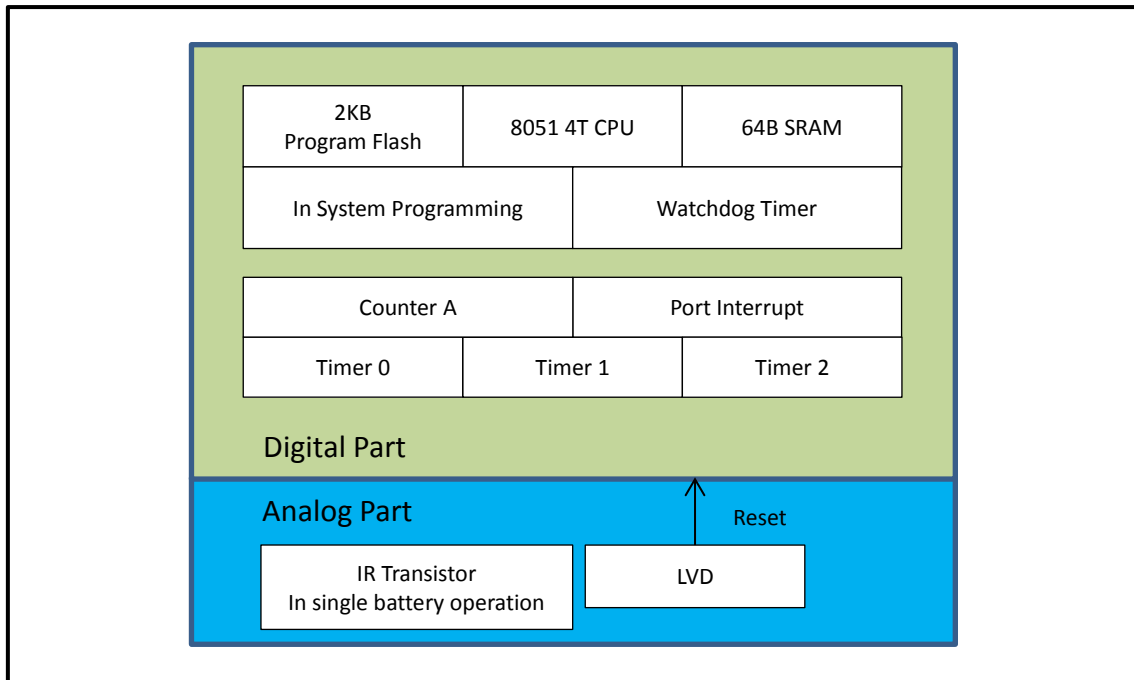
The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

5 Architecture

With the 4T 8051 8-bit CPU, instruction execution time is 500ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

The block diagram is illustrated in the following figure.



6 Central Processing Unit (CPU)

The 4T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

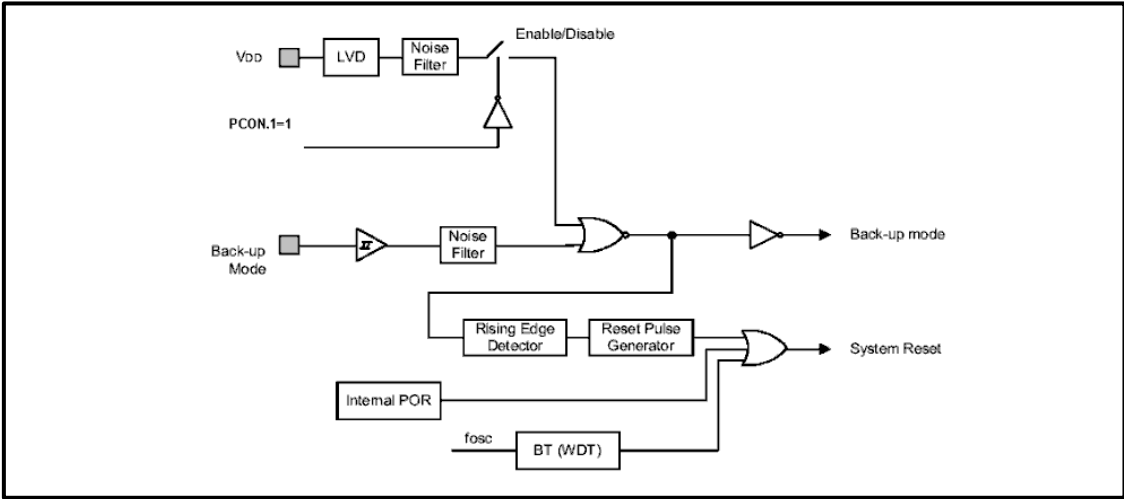
7 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1} , the IC goes into back-up mode at the moment " $V_{DD} = V_{LVD1}$ ".

On the other hand, system reset pulse is generated by the rising slope of V_{DD} . While the voltage at pin

V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment " $V_{DD} \geq V_{LVD2}$ ".

LVD provides a hysteresis ($V_{LVD2} - V_{LVD1}$) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.

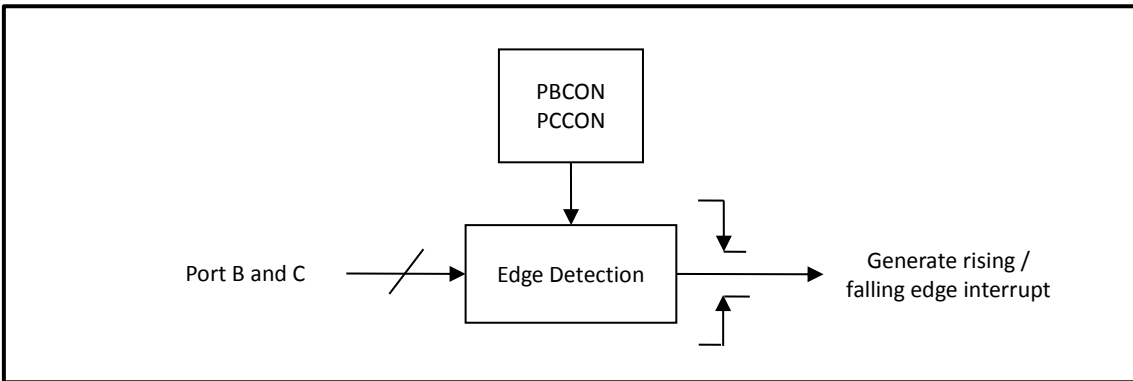


8 I/O port

The 20-pin package has one 8-bit port (PA), one 4-bit port (PB) and one 3-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (11111111). Port C is set to the value (00001101).

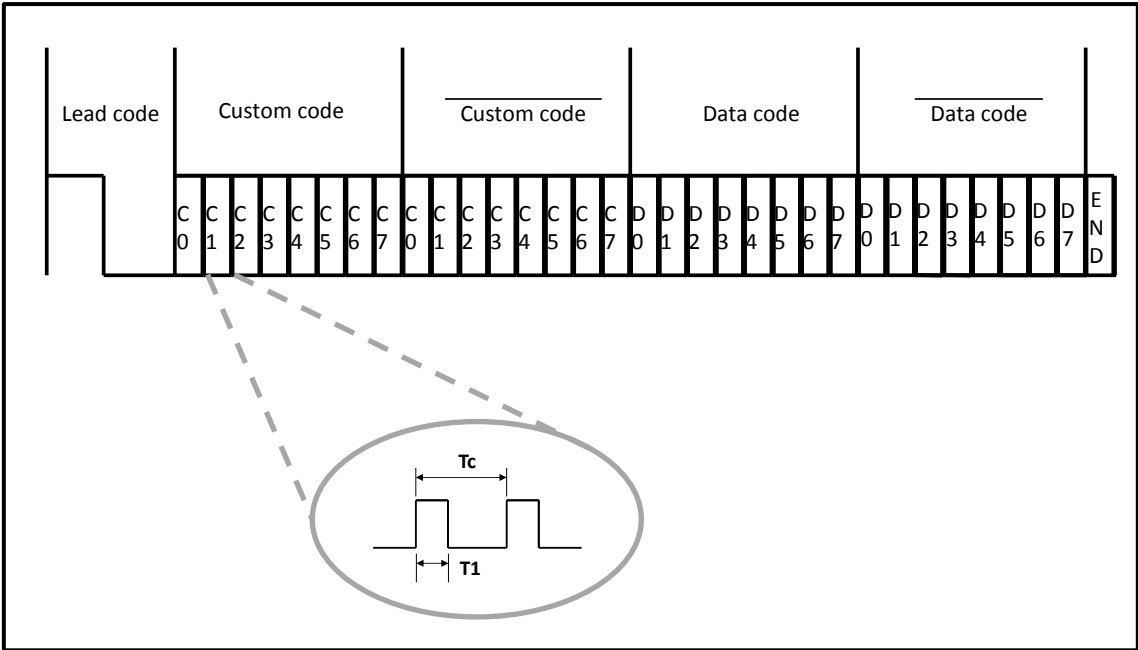
The 16-pin package has one 4-bit port (PA), one 4-bit port (PB) and one 3-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (11111111). Port C is set to the value (00001101).

Port interrupt function is supported for port B and C. Pull-up resistors are also included and could be assigned pin-by-pin by programming the pull-up resistor enable register.



9 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

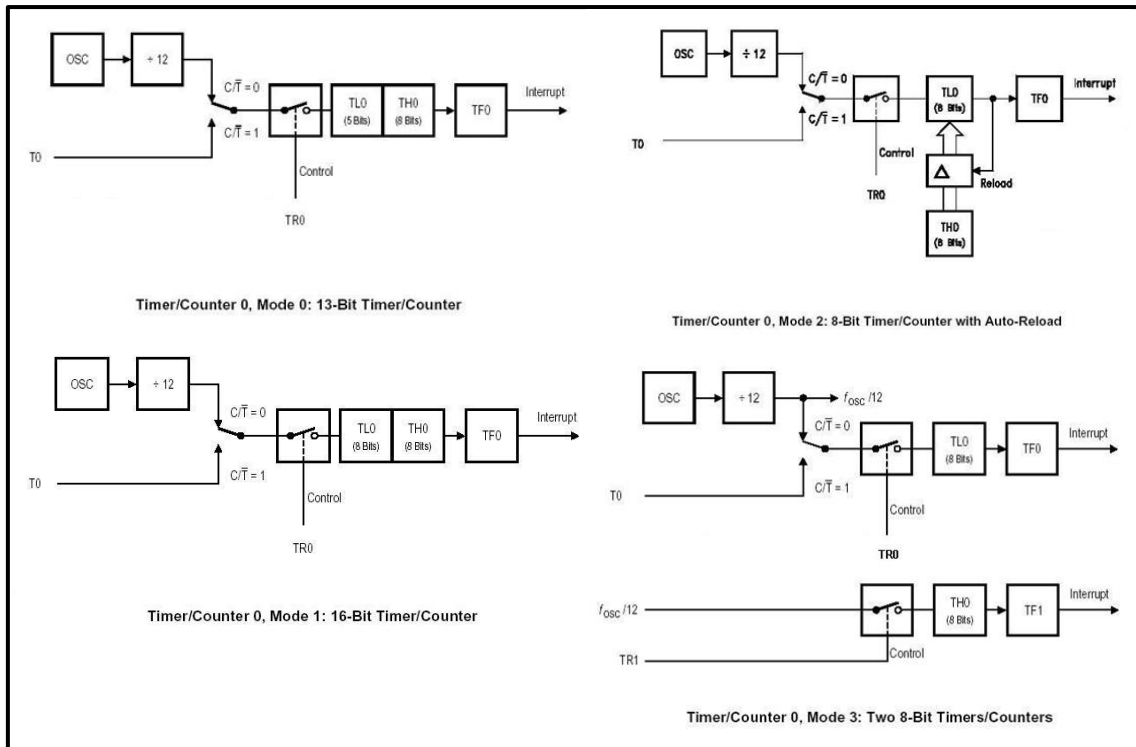
10 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the ‘timer’ function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the ‘counter’ function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.

- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



11 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires only 3 wires to minimize the number of added components and board area impact.

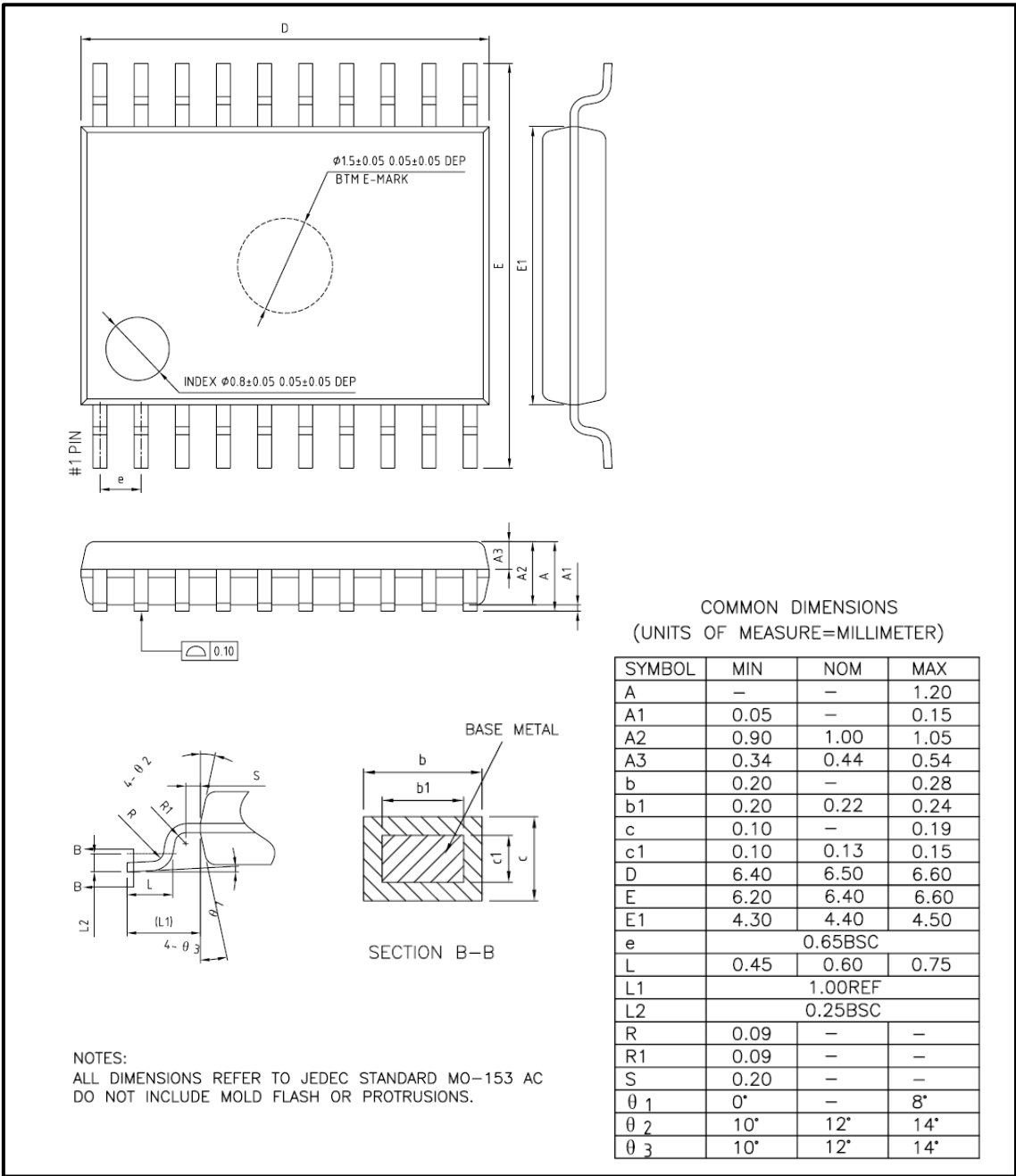
12 Ordering Information

| Part No | Package | Program Flash | Data Flash | SRAM | I/O |
|------------------|------------|---------------|------------|------|-----|
| DC6688F2SEN | TSSOP20 | 2KB | - | 64B | 16 |
| DC6688F2SEN-TR1 | TSSOP20[1] | 2KB | - | 64B | 16 |
| DC6688F2SENP | SSOP20 | 2KB | - | 64B | 16 |
| DC6688F2SENP-TR1 | SSOP20[1] | 2KB | - | 64B | 16 |
| DC6688F2SEK | SOP16 | 2KB | - | 64B | 12 |

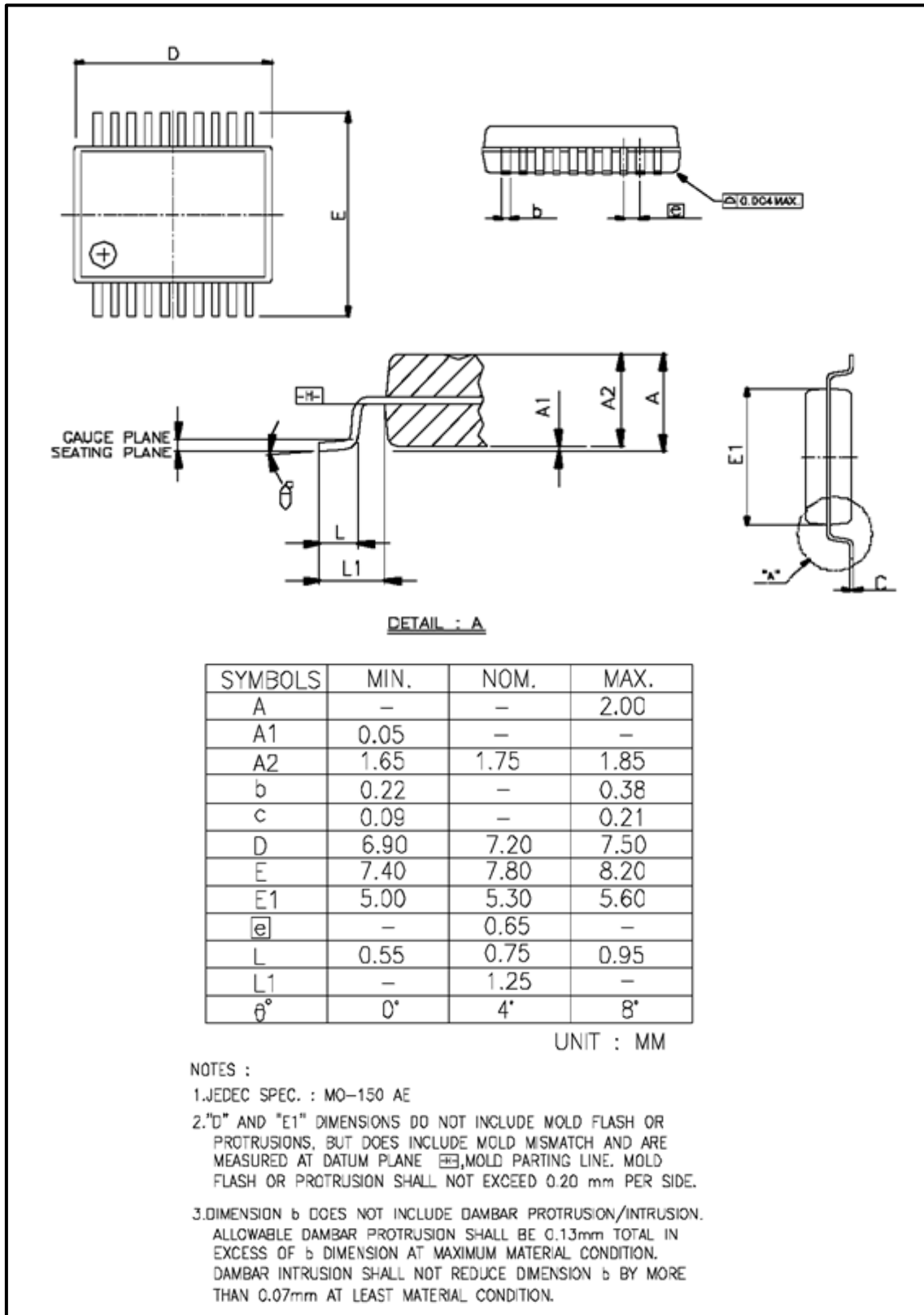
[1] Tape and reel packing.

13 Package Outlines

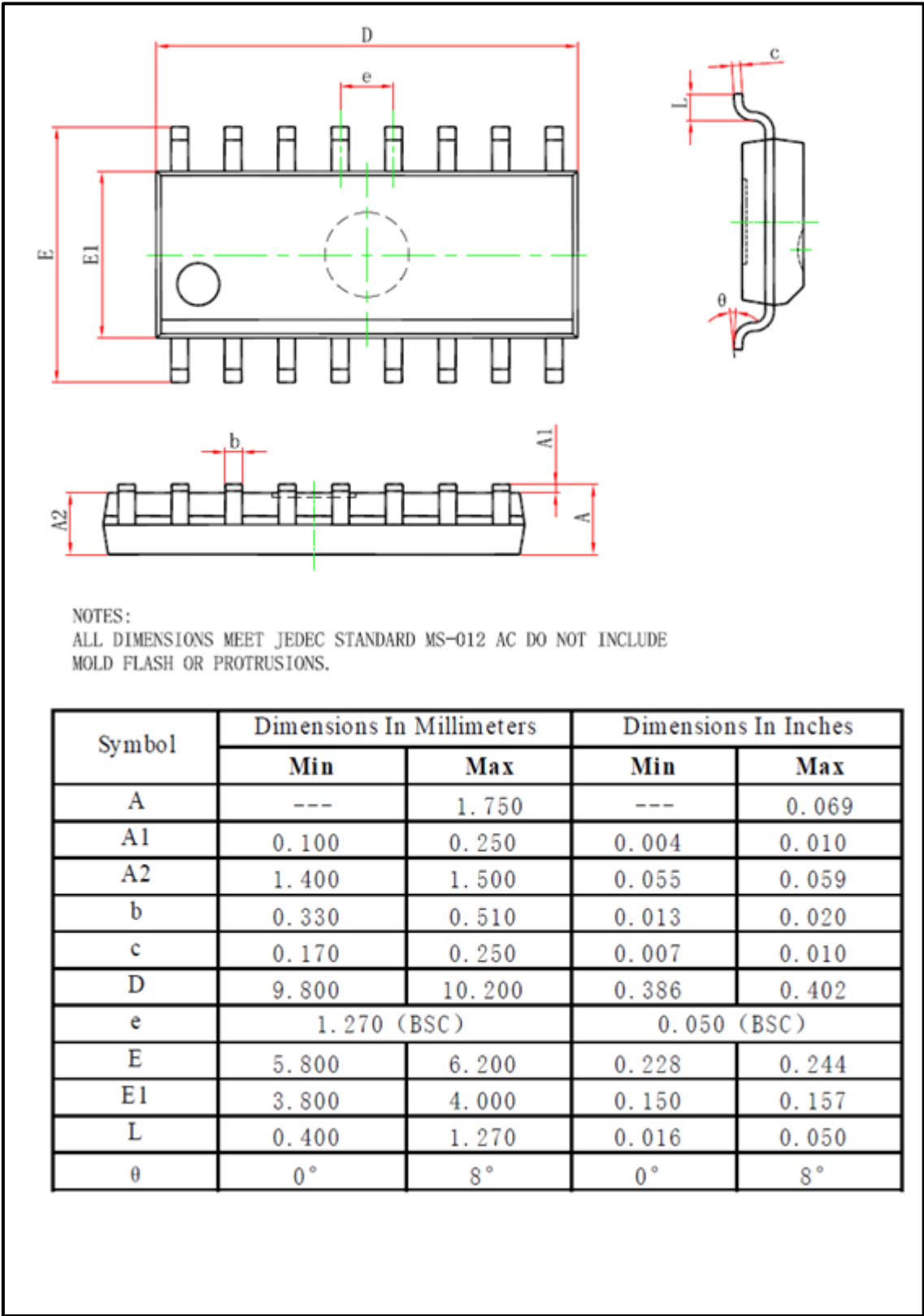
13.1 20-pin TSSOP



13.2 20-pin SSOP



13.3 16-pin SOP



14 Revision History

| Document Rev No. | Issued Date | Section | Page | Description | Edited by | Reviewed by |
|------------------|-------------|---------|------|---|-------------|-------------|
| 0.9 | Feb, 2012 | - | - | Preliminary release | Celia Ki | Danny Ho |
| 0.9a | April, 2012 | - | - | Revise the Idd measuring condition to VDD=1.5V | Celia Ki | Danny Ho |
| 1.0 | March, 2013 | - | - | Update for new features: Remove UART and SPI section | Celia Ki | Danny Ho |
| 1.3 | May, 2014 | - | - | Add IR Transistor configuration | Celia Ki | Danny Ho |
| 1.4 | March, 2014 | - | - | Change the operating voltage | Philip Hung | Fred Law |
| 1.5 | April, 2014 | - | - | Add SOP 16 package | Philip Hung | Eddy Cheung |
| 1.6 | May, 2014 | - | - | Release new format | Philip Hung | Kennis To |
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Dragonchip Ltd.

TEL: (852) 2776-0111

FAX: (852) 2776-0996

<http://www.dragonchip.com>