DC6688FLT

Super 1T 8051 Microcontroller

DC6688FLT is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Power Down and Backup modes
- Memory
  - 16KB/32KB/64KB/96KB Configurable Program & Data Flash Memory
  - Security bit for read back protection
  - Internal 256B SRAM; Expanded 1.5KB/3KB SRAM
- Internal 12MHz/16MHz oscillator
  - ± 1% accuracy from -20°C to +70°C, V_{DD} = 2.0V to 3.6V (FL16T/FL32T)
  - ± 1% accuracy from -20°C to +70°C, V_{DD} = 1.8V to 3.6V (FL64T/FL96T)
- Built-in transistor for IR LED (I_{OL} = 300mA at V_{OL} = 0.5V)
- IR generator by counter A with auto-reload function
- Built-in IR amplifier and a 24-bit Timer for learning module
- Dedicated input pin for IR learning
- Code executes from SRAM
- 4-level priority interrupt controller
- 25 bit-programmable I/O ports
- 16-bit Timers x 3
- 8-bit PWM Timer x 2
- Standard UART x 2
- SPI Master
- I2C Master/Slave
- Low Voltage Detection (LVD) for backup mode
- Low Voltage Indication (LVI) - Programmable
- Maximum operating voltage: 3.6V
- Operating temperature: -40°C to +85°C
- Package type:
  - 8-pin TSSOP
  - 16-pin SOP
  - 16-pin SSOP
  - 20-pin QFN
  - 20-pin TSSOP
  - 24-pin TSSOP
  - 28-pin TSSOP
  - Bare die

Quick look on Ordering Information

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B,C and D[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B,C and D[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:
[1] It is measured for any one of I/O pin when configured to push-pull output high.
[2] It is measured as total for Ports A, B, C and D when configured to push-pull output high.
[3] It is measured for any one of I/O pin when configured to push-pull output low.
[4] It is measured as total for Ports A, B, C and D when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz/16MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH1}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input pins	0	-	0.3 V_{DD}	V
Output High Voltage	V_{OH1}	Port C1, V_{DD} = 2.4V, I_{OH} = - 6mA, T_A = 25°C	V_{DD} – 0.7	-	-	V
	V_{OH2}	Port C0, C2, C3, C4, C5, V_{DD} = 2.4V, I_{OH} = - 2.2mA, T_A = 25°C	V_{DD} – 0.7	-	-	V
	V_{OH3}	All output pins except Port C pins, V_{DD} = 2.4V, I_{OH} = - 1mA, T_A = 25°C	V_{DD} – 1.0	-	-	V
Output Low Voltage	V_{OL1}	Port C1, V_{DD} = 2.4V, I_{OL} = 12mA, T_A = 25°C	-	0.4	1	V
	V_{OL2}	Port C0 & C2, V_{DD} = 2.4V, I_{OL} = 12mA, T_A = 25°C	-	0.4	1	V
	V_{OL3}	All output pins except Port C pins, V_{DD} = 2.4V, I_{OL} = 1mA, T_A = 25°C	-	0.4	1	V
Output Low Current IR Transmit	$I_{OL(IRTX)}$	V_{OL} = 0.5V, IRDRV = 3, T_A = 25°C	-	300	-	mA
Input High Leakage Current	I_{LIH1}	All input pins except PROG, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH3}	PROG, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins, V_{IN} = 0	-	-	-1	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	40	80	160	kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull-down Resistors [3]	R_{PD}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Supply Current Run Mode [1]	Idd(op)	f_{OSC} = 12MHz/16MHz, V_{DD} = 3.0V, T_A = 25°C	-	2	8	mA
Supply Current Power Down Mode [2]	Idd(pd)	V_{DD} = 3.0V, Bit 7(T24_CON1) = 0, T_A = 25°C	-	2	5	µA
Supply Current Power Down Mode with T-scan [2]	Idd(pdt)	V_{DD} = 3.0V, T-scan inactive period = 81.92ms, Bit 7(T24_CON1) = 0, T_A = 25°C	-	3	-	µA

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is tested if the condition is that:

a) Port A output open-drain.

b) Port B and C input enable pull-up resistor.

c) Port C1 output push-pull.

d) Port D output push-pull.

[3] For DC6688FL64T/FL96T

1.3 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Program setting	1.65	1.8	1.95	V
		Default setting	2.0	2.15	2.3	V
		Program setting	2.35	2.5	2.65	V
		Program setting	2.65	2.8	2.95	V
Low Voltage Detect Level	V_{LVD1}	DC6688FL64T/96T	1.4	1.5	1.6	V
		DC6688FL16T/32T	1.5	1.6	1.7	V

Remarks:

[1] $V_{LVD2} - V_{LVD1} = \Delta V$

1.4 SRAM Data Retention Voltage

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Current	I_{DDDR}	V_{DDDR} = 1.0V, Stop mode	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.7 Oscillation Characteristics

Oscillator	Conditions	Min	Typ	Max	Unit
Internal 12MHz/16MHz Oscillator	T_A = -20°C to +70°C, V_{DD} = 2.0V to 3.6V (FL16T/FL32T) V_{DD} = 1.8V to 3.6V (FL64T/FL96T)	-	-	± 1%	MHz
Internal 50kHz Oscillator	T_A = -20°C to +70°C	-	50	-	kHz

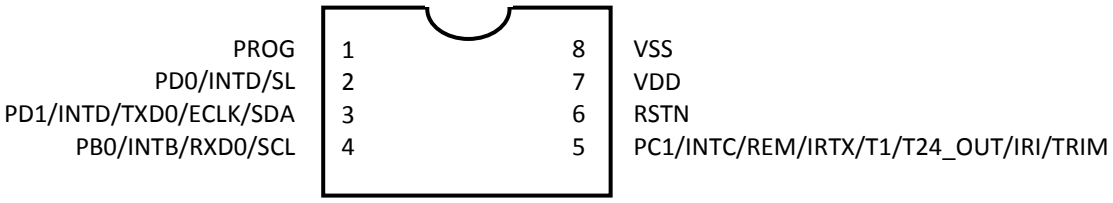
(T_A = -40°C to +85°C, V_{DD} = 3.0V)

Parameter	Conditions	Min	Typ	Max	Unit
Oscillator Stabilization Wait Time	tWAIT when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
	tWAIT when released by an external interrupt[2]	-	$2^{13}/f_{OSC}$	-	ms

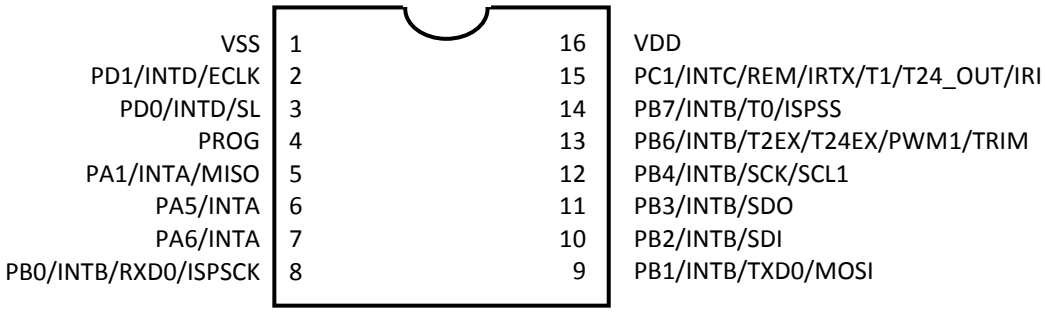
Remarks:
[1] f_{osc} is the oscillator frequency.
[2] The duration of the oscillation stabilization time(tWAIT) when it is released from power down mode by PA or PB interrupt.

2 Pin Assignment

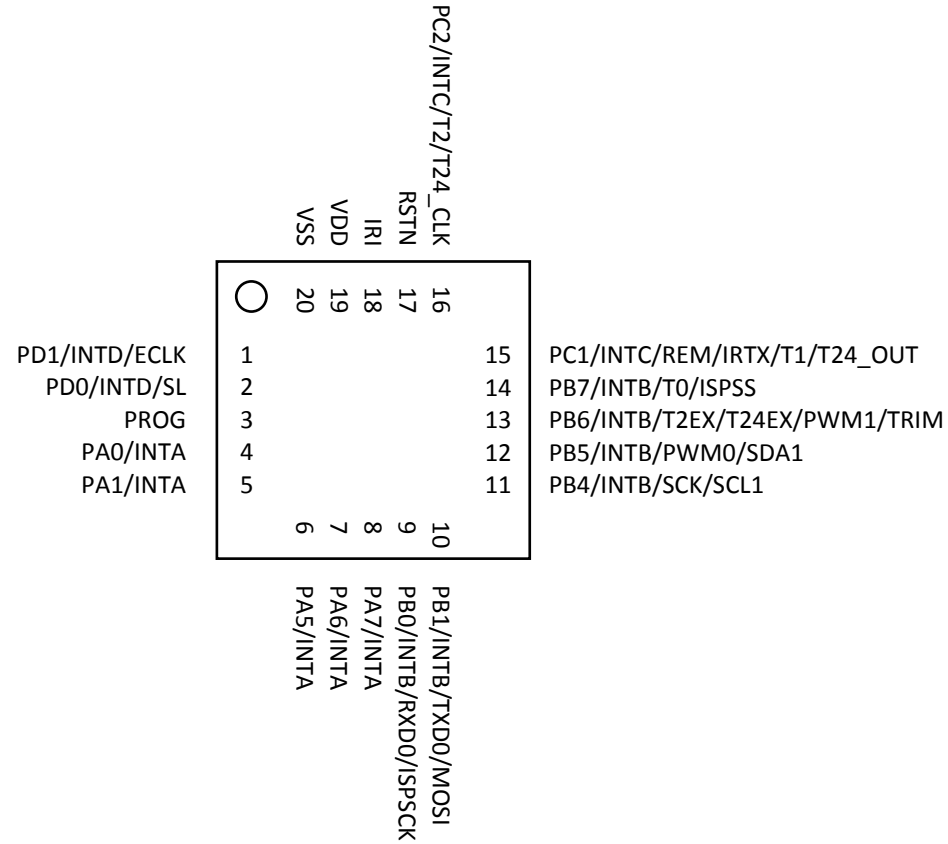
(TSSOP8)



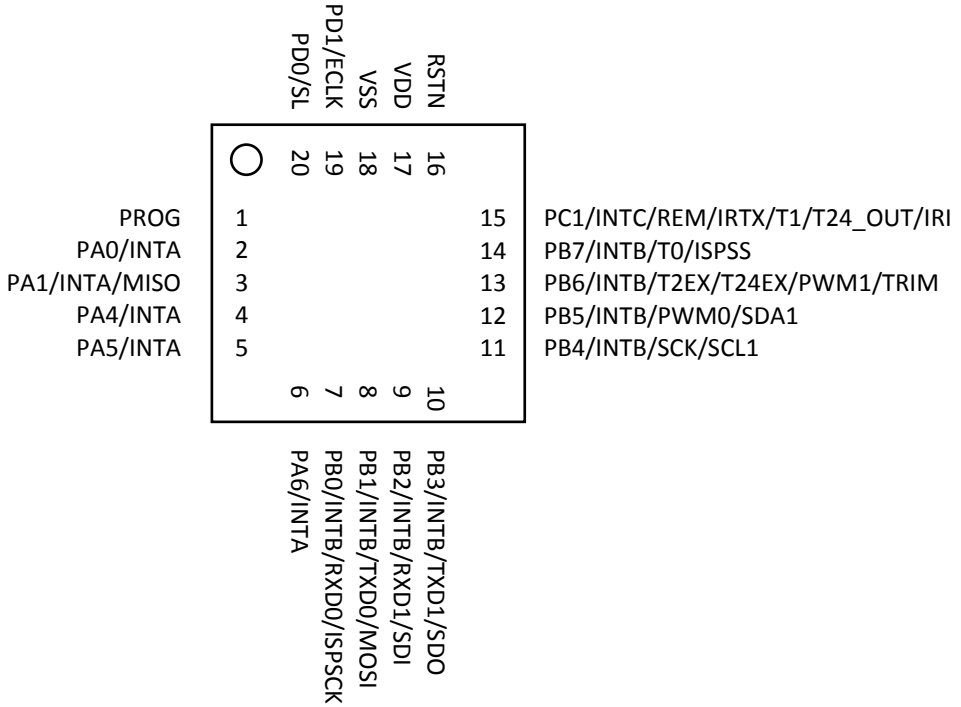
(SOP16 / SSOP16)



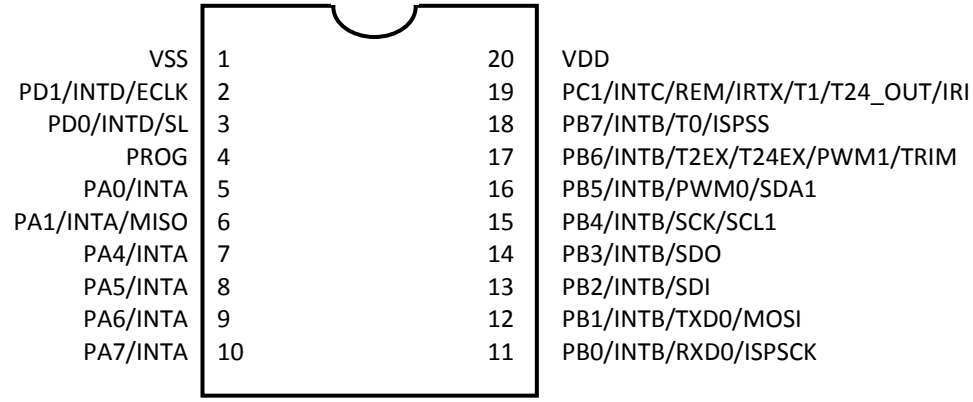
(QFN20 – DC6688FL32TQ)



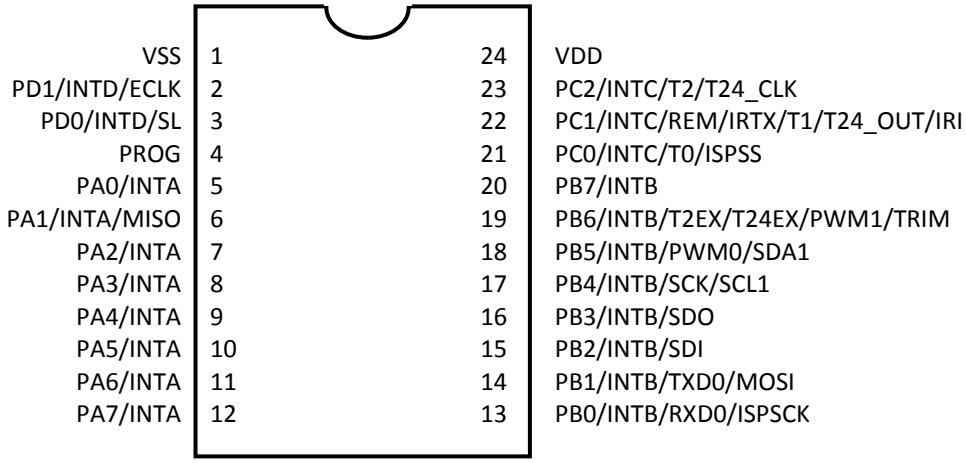
(QFN20 – DC6688FL96TQ)



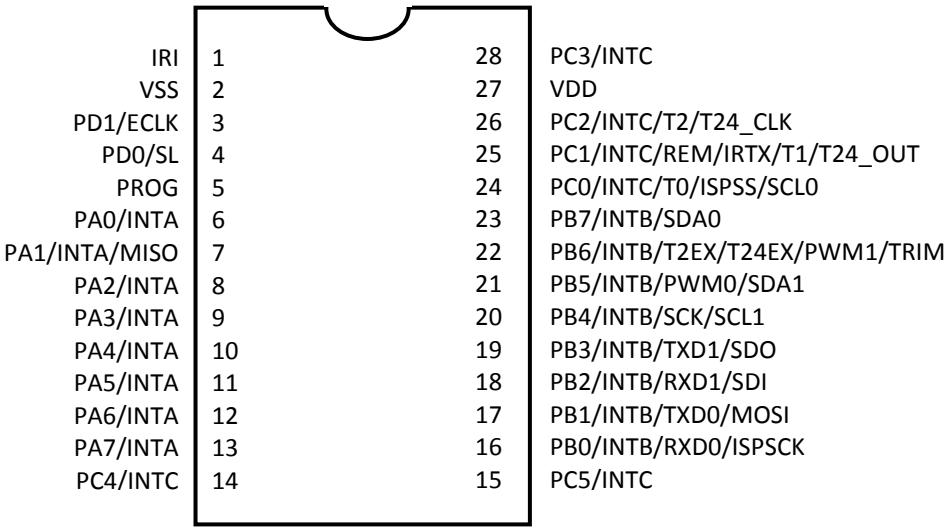
(TSSOP20)



(TSSOP24)



(TSSOP28)



TSSOP8	SOP16 SSOP16	QFN20 (FL32T)	QFN20 (FL96T)	TSSOP20	TSSOP24	TSSOP28	Pin Name	Symbol	Function
5	15	18	15	19	22	1	IRI	IRI	Infrared signal input
1	4	3	1	4	4	5	PROG	PROG	Programming select
6	-	17	16	-	-	-	RSTN	RSTN	Reset
7	16	19	17	20	24	27	VDD	VDD	Power
8	1	20	18	1	1	2	VSS	VSS	Ground
-	-	4	2	5	5	6	PA0/INTA	PA0	Configurable input or output port
								INTA	Port interrupt input
-	5	5	3	6	6	7	PA1/INTA/MISO	PA1	Configurable input or output port
								INTA	Port interrupt input
								MISO	ISP Master In Slave Out
-	-	-	-	-	7	8	PA2/INTA	PA2	Configurable input or output port
								INTA	Port interrupt input
-	-	-	-	-	8	9	PA3/INTA	PA3	Configurable input or output port
								INTA	Port interrupt input

TSSOP8	SOP16 SSOP16	QFN20 (FL32T)	QFN20 (FL96T)	TSSOP20	TSSOP24	TSSOP28	Pin Name	Symbol	Function
-	-	-	4	7	9	10	PA4/INTA	PA4	Configurable input or output port
								INTA	Port interrupt input
-	6	6	5	8	10	11	PA5/INTA	PA5	Configurable input or output port
								INTA	Port interrupt input
-	7	7	6	9	11	12	PA6/INTA	PA6	Configurable input or output port
								INTA	Port interrupt input
-	-	8	-	10	12	13	PA7/INTA	PA7	Configurable input or output port
								INTA	Port interrupt input
4	8	9	7	11	13	16	PB0/INTB/RxD0 /ISPSCK/SCL	PB0	Configurable input or output port
								INTB	Port interrupt Input
								RxD0	UART receiver data input
								ISPSCK[5]	ISP serial clock
								SCL[4]	I2C master/slave serial clock
-	9	10	8	12	14	17	PB1/INTB/TxD0 /MOSI	PB1	Configurable input or output port
								INTB	Port interrupt input
								TxD0	UART transmitter data output
								MOSI	ISP master out slave in
-	10	-	9	13	15	18	PB2/INTB/RxD1 /SDI	PB2	Configurable input or output port
								INTB	Port interrupt input
								RxD1[2]	UART receiver data input
								SDI	SPI Serial Data In
-	11	-	10	14	16	19	PB3/INTB/TxD1 /SDO	PB3	Configurable input or output port
								INTB	Port interrupt input
								TxD1[2]	UART transmitter data output
								SDO	SPI serial data out
-	12	11	11	15	17	20	PB4/INTB/SCK/S CL1	PB4	Configurable input or output port
								INTB	Port interrupt input
								SCK	SPI serial clock
								SCL1	I2C master/slave serial clock
-	-	12	12	16	18	21	PB5/INTB/PWM 0/SDA1	PB5	Configurable input or output port
								INTB	Port interrupt input
								PWM0	PWM output
								SDA1	I2C master/slave serial data
-	13	13	13	17	19	22	PB6/INTB/T2EX/ T24EX/PWM1/T RIM	PB6	Configurable input or output port
								INTB	Port interrupt input
								T2EX	Timer 2 capture-reload trigger / up down count
								T24EX	T24 timer capture-reload trigger
								PWM1	PWM output
								TRIM	Clock trimming
-	14	14	14	18	20	23	PB7/INTB/SDA0 /T0/ISPSS	PB7	Configurable input or output port
								INTB	Port interrupt input
								SDA0[2]	I2C master serial data
								T0[1]	Timer 0 external counter input
								ISPSS[1]	ISP slave select
-	-	-	-	-	21	24	PC0/INTC/T0/IS PSS/SCL0	PC0	High current drive configurable I/O
								INTC	Port interrupt input
								T0	Timer 0 external counter input
								ISPSS	ISP slave select
								SCL0[2]	I2C master serial clock
5	15	15	15	19	22	25	PC1/INTC/REM/ IRTX/T1/T24_O	PC1	High current drive configurable I/O
								INTC	Port interrupt input

TSSOP8	SOP16 SSOP16	QFN20 (FL32T)	QFN20 (FL96T)	TSSOP20	TSSOP24	TSSOP28	Pin Name	Symbol	Function
							UT/TRIM	REM	Counter A carrier frequency output
								IRTX	IR Transmit with built-in transistor
								T1	Timer 1 external counter input
								T24_OUT	T24 timer clock output
								TRIM[4]	Clock trimming
-	-	16	-	-	23	26	PC2/INTC/T2/T24_CLK	PC2	High current drive configurable I/0
								INTC	Port interrupt input
								T2	Timer 2 external counter input
								T24_CLK	Timer 2 clock Output
-	-	-	-	-	-	28	PC3/INTC	PC3	High current drive configurable I/0
								INTC	Port Interrupt Input
-	-	-	-	-	-	14	PC4/INTC	PC4	High current drive configurable I/0
								INTC	Port Interrupt Input
-	-	-	-	-	-	15	PC5/INTC	PC5	High current drive configurable I/0
								INTC	Port Interrupt Input
2	3	2	20	3	3	4	PD0/INTD/SL	PD0	High current drive configurable I/0
								INTD[3]	Port Interrupt Input
								SL	SL (Single Line) communication signal
3	2	1	19	2	2	3	PD1/INTD/TXD0/ECLK/SDA	PD1	High current drive configurable I/0
								INTD[3]	Port Interrupt Input
								TXD0[4]	UART transmitter data output
								ECLK	External clock for programming
								SDA[4]	I2C master/slave serial data

Remarks:
[1] Only for 16pin and 20pin package
[2] Only for DC6688FL64T/FL96T
[3] Only for DC6688FL16T/FL32T
[4] Only for 8pin package
[5] Not for 8pin package

3 Description

DC6688FLT is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory. Internal RC oscillator is equipped, generating 16MHz, 12MHz, 4MHz and 1MHz machine clock without any external components.

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) for IR remote controller application. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

4 Memory

Memory comprises of the following elements, namely:

- 16KB/32KB/64KB/96KB Program Flash memory + Data Flash memory
- 256B Internal SRAM
- 1.5KB/3KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

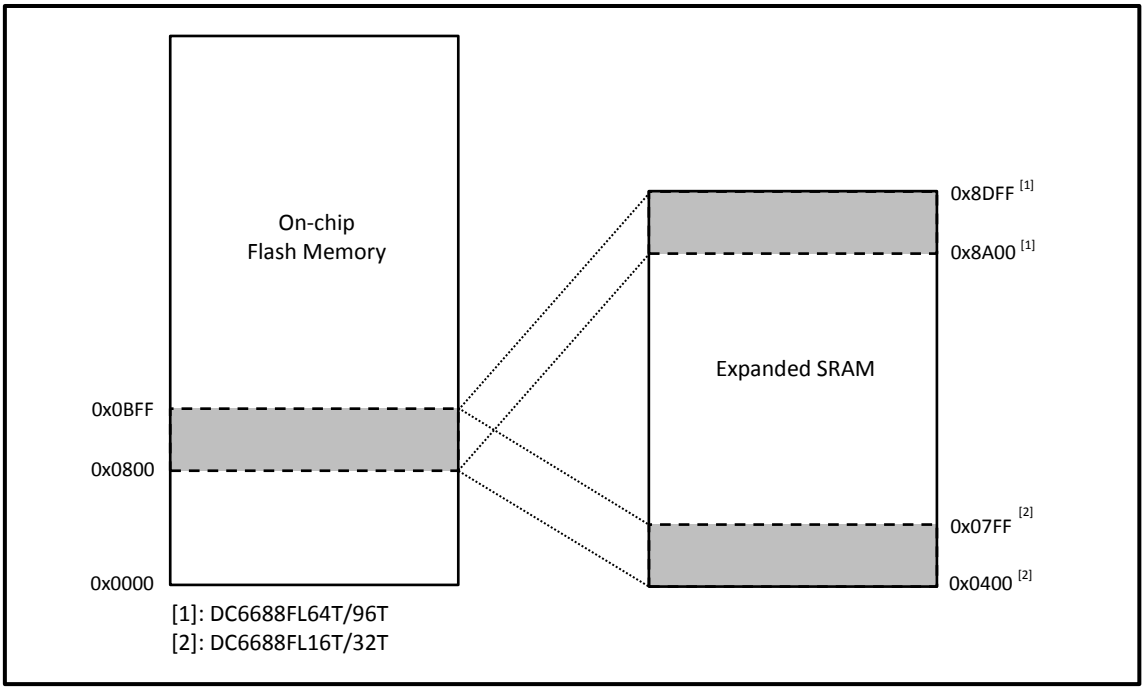
4.1 Program & Data Flash Memory

On-chip program Flash size is configurable, range from 2560 bytes to 97280 bytes, upon different application. It can be programmed by In-System-Programming (ISP) method.

In addition, write protection signature is available to avoid writing accidentally.

4.2 Code Executable from SRAM

Code execution enables the mapping of Flash memory to SRAM. This SRAM segment replaces the on-chip Flash memory.



4.3 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, UART, etc. Some locations in the SFR address space are addressable as bits.

4.4 External Function Register (XFR)

The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

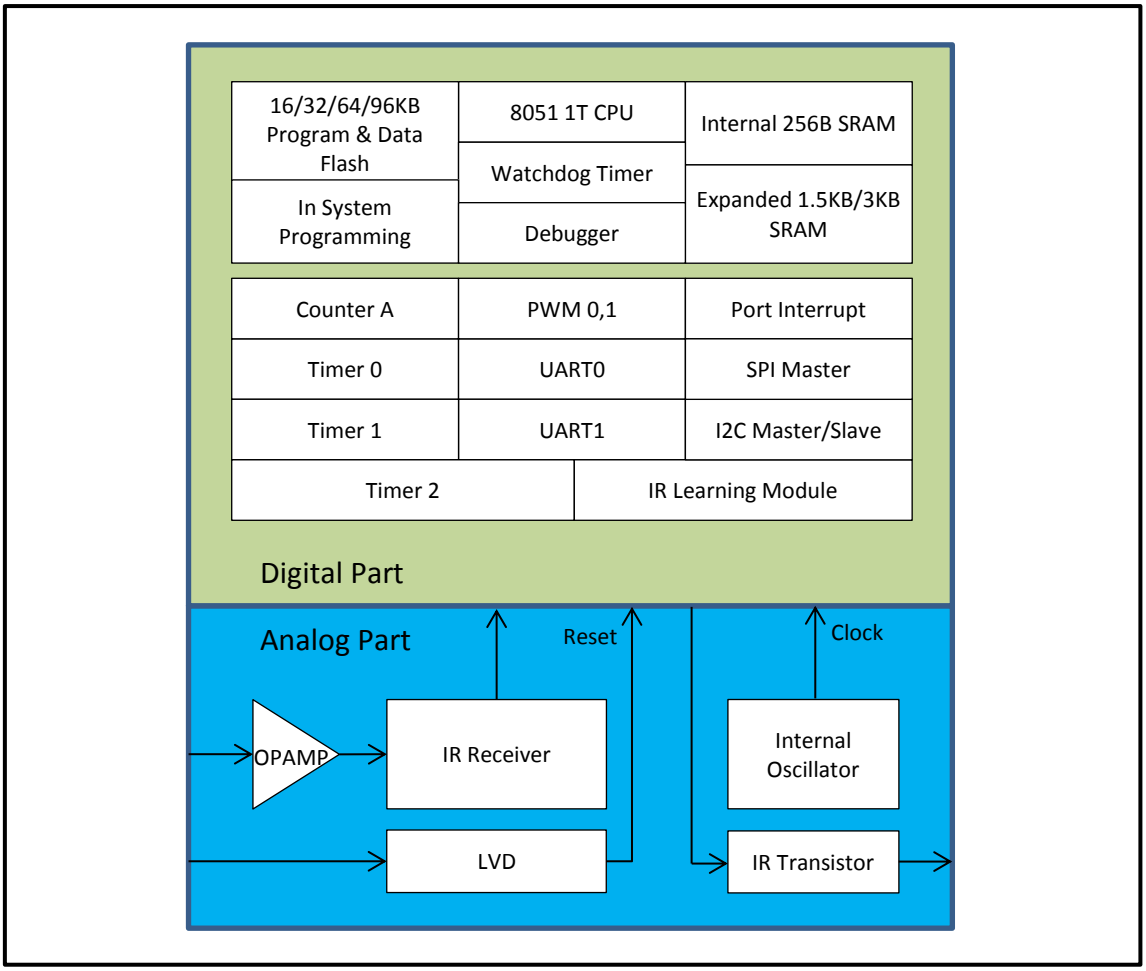
5 Architecture

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

Internal RC oscillator is equipped and operated at 16MHz, 12MHz, 8MHz, 6MHz, 4MHz, 2MHz and 1MHz software selectable without external components. It supports trimming by In-System Programmer to ensure the oscillator within specification.

The block diagram is illustrated in the following figure.



6 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

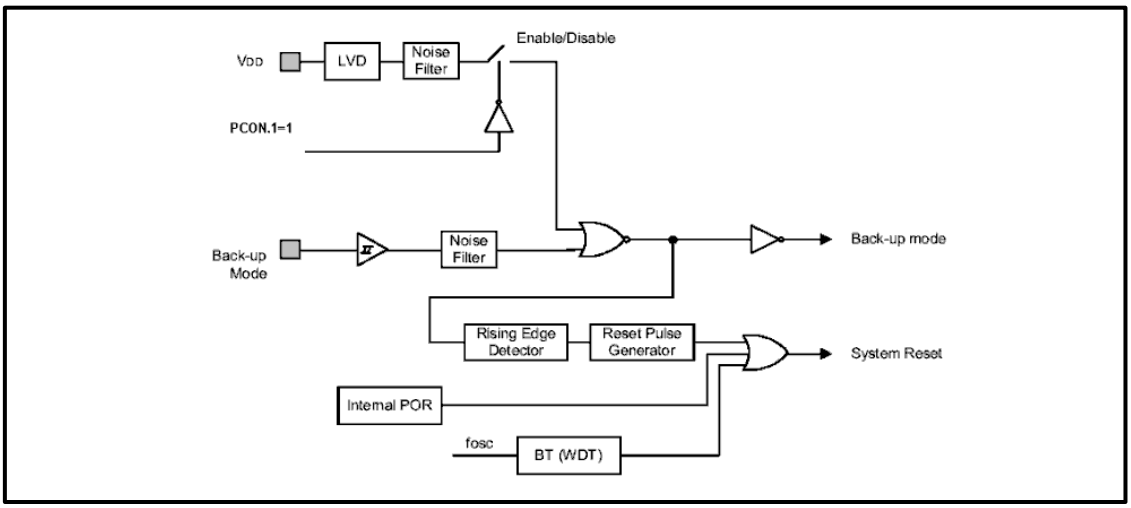
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

7 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



8 I/O port

The 8-pin package has one 7-bit port (PB), one 1-bit port (PORTC) and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

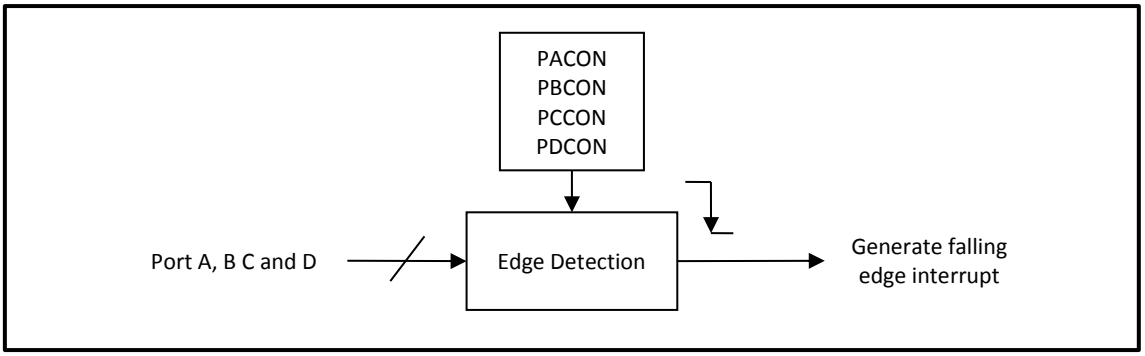
The 16-pin package has one 3-bit port (PA), one 7-bit port (PB), one 1-bit port (PORTC) and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

The 20-pin package has one 6-bit port (PA), one 8-bit ports (PB), one 1-bit port (PORTC) and one 1-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

The 24-pin package has two 8-bit ports (PA and PB), one 2-bit port (PORTC) and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

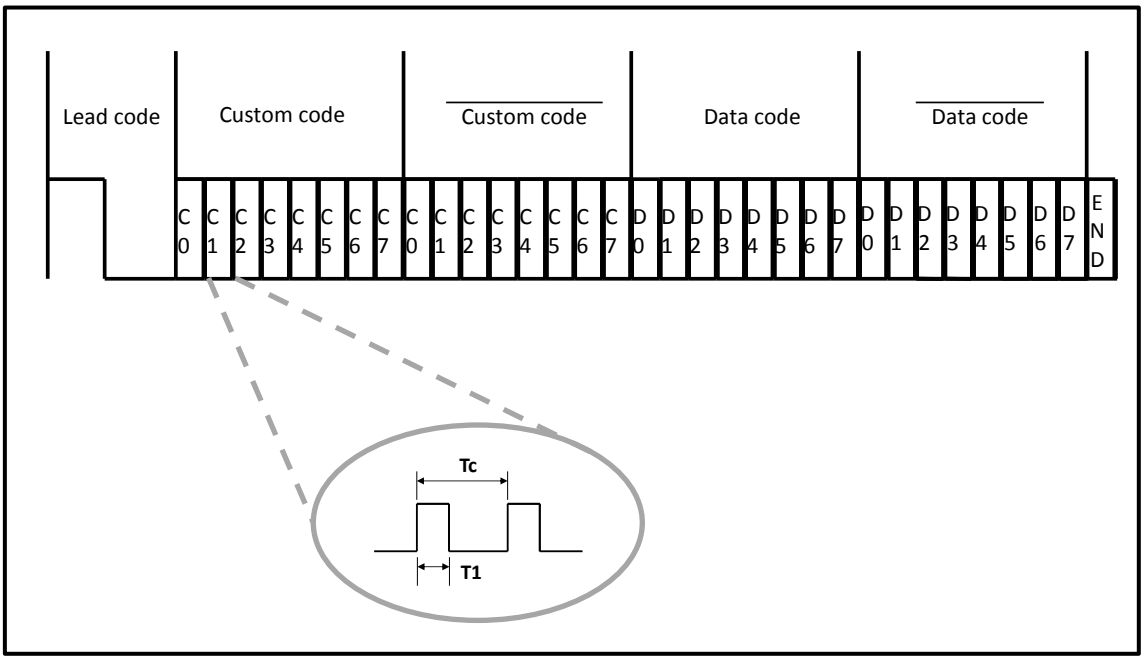
The 28-pin package has two 8-bit ports (PA and PB) and one 6-bit port (PORTC) and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

Port interrupt function is supported for port A, B, C and D. Pull-up resistors are also included and could be assigned pin-by-pin by programming the pull-up resistor enable register.



9 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

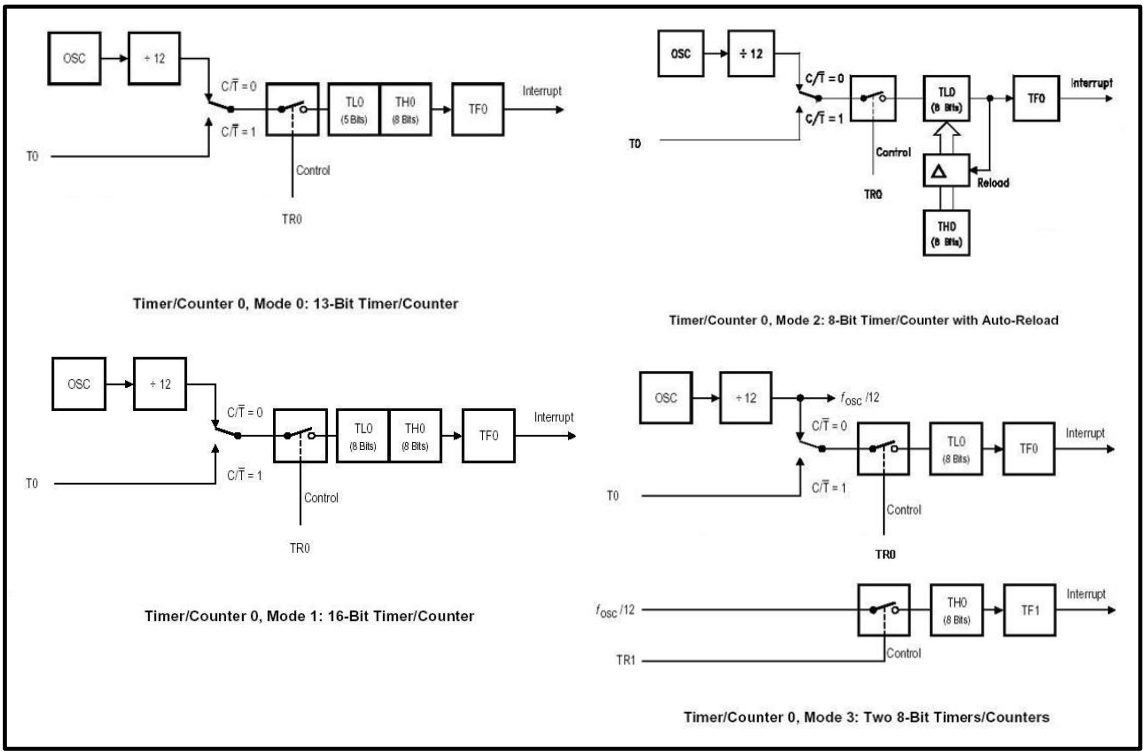
10 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no

restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



11 Enhanced UART

The UART operates in all of the usual modes and perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

The full duplex UART ports are able to transmit and receive simultaneously. These serial ports are also receive-buffered. It can commence reception of a second byte before the previously received byte has been read from the receive register. If, however, the first byte has still not been read by the time reception of the second byte is complete, one of the bytes will be lost. The SIO receive and transmit registers are both accessed via the SBUF special function register. Writing to SBUF loads the transmit register, and reading SBUF accesses to a physically separate receive register. SIO can operate in 4 modes.

The UART operates in four modes (one synchronous and three asynchronous). The Serial 0 is buffered at the receive side, i.e. it can receive new data while the previously received is not damaged in the receive register until the completion of the 2nd transfer.

The UART is fully compatible with the standard 8051 serial channel.

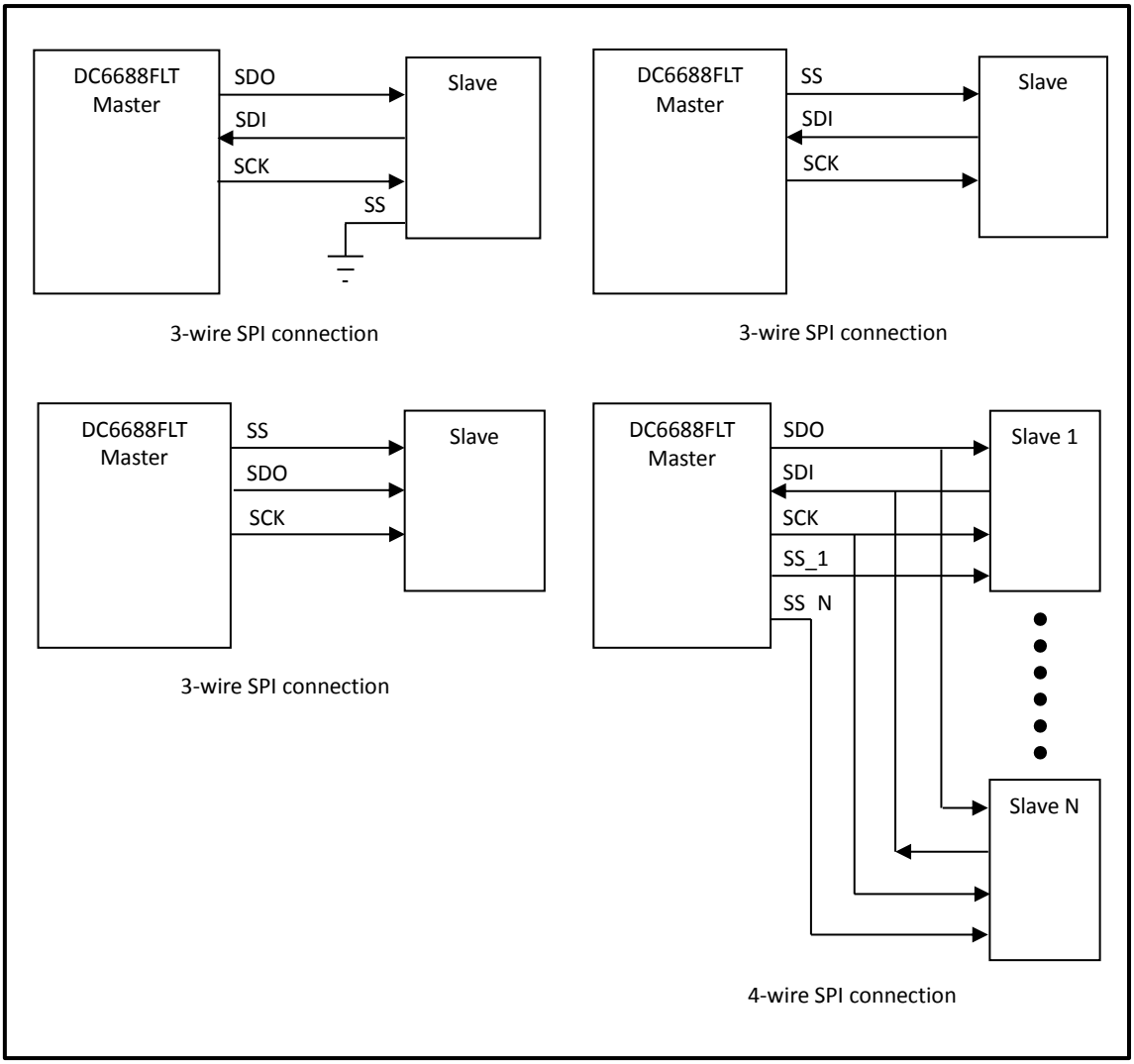
12 Serial Peripheral Interface

A complete hardware Serial Peripheral Interface (SPI) on-chip in master mode is integrated. SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously.

The SPI interface consists of the following wires:

- SDI
  The SDI line on the master (data in) should be connected to the SDO/MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.
- SDO
  The SDO line on the master (data out) should be connected to the SDI/MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.
- SCK
  The master serial clock (SCK) is used to synchronize the data being transmitted and received through the SDO and SDI data lines. A single data bit is transmitted and received in each SCK period. Therefore, a byte is transmitted/received after eight SCK periods.
- SS
  In the slave device, SPI interface requires the slave select line (SS) to enable communication such that DC6688FLT (master) can talk to more than one slave device in different time slot. To be able to talk to the slave device, master should assert the SS pin on an external slave device. This can be done by using a Port digital output pin which is manually controlled by software.

The hardware connection methods are shown below.



13 Inter-Integrated Circuit (I2C) Interface

The I2C Bus Controller supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: “SCL” (serial clock line) and “SDA” (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus.

The interface defines 2 transmission speeds if 12MHz crystal is used:
- Normal: 100Kbps
- Fast: 400Kbps

The I2C component performs 8-bit-oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode and may operate in the two modes.

Mode	Description
Master Transmitter Mode	Serial data output through SDA while SCL output the serial clock.
Master Receiver Mode	Serial data is received via SDA while SCL outputs the serial clock.
Slave Receiver Mode	Serial data and the serial clock and received through SDA and SCL
Slave Transmitter Mode	Serial data is transmitted via SDA while the serial clock is input through SCL

14 Infrared Learning Module

IR learning module includes IR receiver and T24 timer. Analog signal entering IRI pin is converted to digital signal by IR receiver, and feed to T24 timer.

With the built-in Op Amp circuit, no external amplifier circuit is needed. The high resolution 24-bit timer provides a high capability of IR learning. It can capture carrier frequency as high as 500kHz.

15 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires 6 wires to minimize the number of added components and board area impact.

16 Ordering Information

12MHz internal oscillator:

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688FL32TY	TSSOP8	32KB Configurable		256B + 1.5KB	4
DC6688FL32TY-TR1	TSSOP8[1]	32KB Configurable		256B + 1.5KB	4
DC6688FL16TK	SOP16	16KB Configurable		256B + 1.5KB	13
DC6688FL16TV	SSOP16	16KB Configurable		256B + 1.5KB	13
DC6688FL32TQ	QFN20	32KB Configurable		256B + 1.5KB	17
DC6688FL32TQ-TR1	QFN20[1]	32KB Configurable		256B + 1.5KB	17
DC6688FL32TH	TSSOP20	32KB Configurable		256B + 1.5KB	17
DC6688FL32TH-TR1	TSSOP20[1]	32KB Configurable		256B + 1.5KB	17
DC6688FL32TR	TSSOP24	32KB Configurable		256B + 1.5KB	21
DC6688FL32TR-TR1	TSSOP24[1]	32KB Configurable		256B + 1.5KB	21
DC6688FL32T-COB	Bare die	32KB Configurable		256B + 1.5KB	22
DC6688FL64TH	TSSOP20	64KB Configurable		256B + 3KB	17
DC6688FL64TH-TR1	TSSOP20[1]	64KB Configurable		256B + 3KB	17
DC6688FL64TT	TSSOP28	64KB Configurable		256B + 3KB	25
DC6688FL64TT-TR1	TSSOP28[1]	64KB Configurable		256B + 3KB	25
DC6688FL96TQ	QFN20	96KB Configurable		256B + 3KB	16
DC6688FL96TQ-TR1	QFN20[1]	96KB Configurable		256B + 3KB	16
DC6688FL96TH	TSSOP20	96KB Configurable		256B + 3KB	17
DC6688FL96TH-TR1	TSSOP20[1]	96KB Configurable		256B + 3KB	17
DC6688FL96TR	TSSOP24	96KB Configurable		256B + 3KB	21
DC6688FL96TR-TR1	TSSOP24[1]	96KB Configurable		256B + 3KB	21
DC6688FL96TT	TSSOP28	96KB Configurable		256B + 3KB	25
DC6688FL96TT-TR1	TSSOP28[1]	96KB Configurable		256B + 3KB	25
DC6688FL96T-COB	Bare die	96KB Configurable		256B + 3KB	30

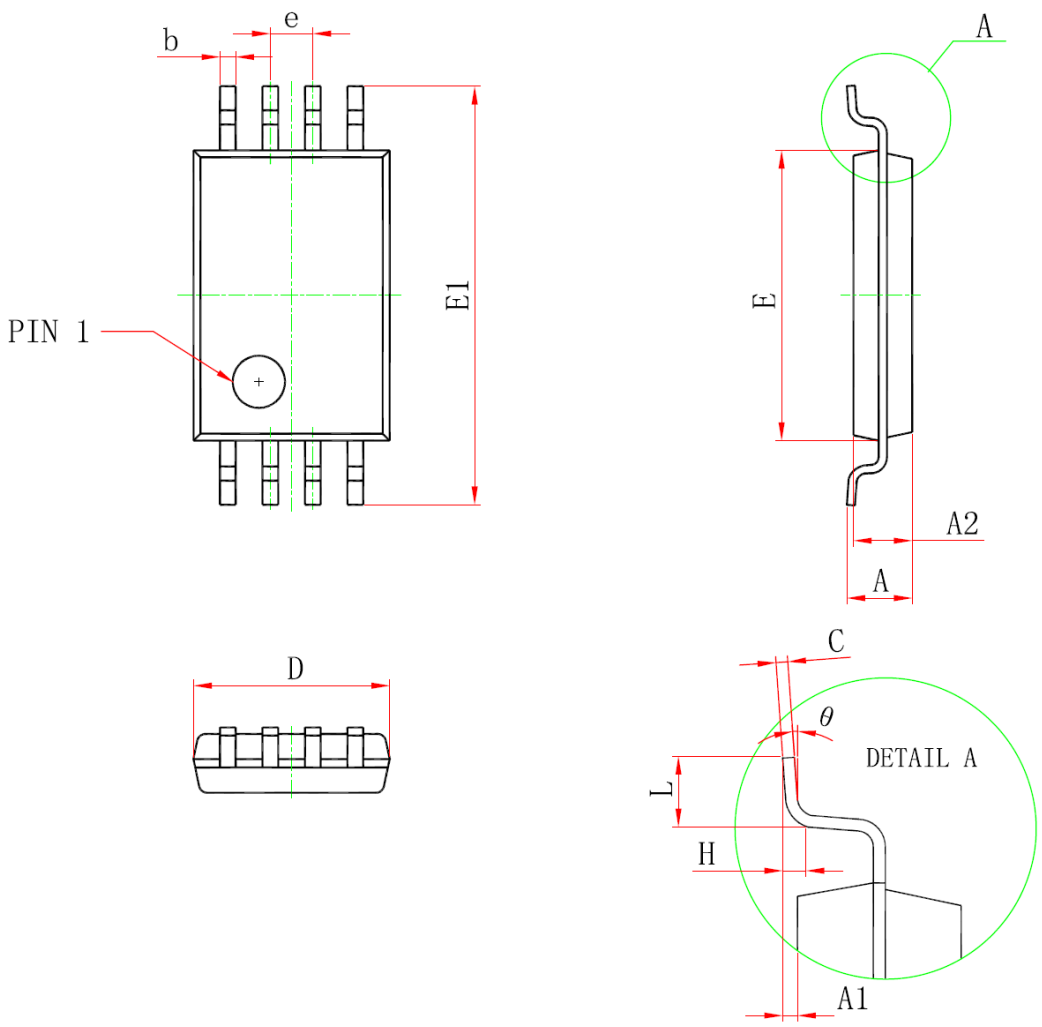
16MHz internal oscillator:

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688FL32TR-16M	TSSOP24	32KB Configurable		256B + 1.5KB	21
DC6688FL32TR-16M-TR1	TSSOP24[1]	32KB Configurable		256B + 1.5KB	21
DC6688FL64TR-16M	TSSOP24	64KB Configurable		256B + 3KB	21
DC6688FL64TR-16M-TR1	TSSOP24[1]	64KB Configurable		256B + 3KB	21
DC6688FL64TT-16M	TSSOP28	64KB Configurable		256B + 3KB	25
DC6688FL64TT-16M-TR1	TSSOP28[1]	64KB Configurable		256B + 3KB	25
DC6688FL96TH-16M	TSSOP20	96KB Configurable		256B + 3KB	17
DC6688FL96TH-16M-TR1	TSSOP20[1]	96KB Configurable		256B + 3KB	17
DC6688FL96TR-16M	TSSOP24	96KB Configurable		256B + 3KB	21
DC6688FL96TR-16M-TR1	TSSOP24[1]	96KB Configurable		256B + 3KB	21
DC6688FL96TT-16M	TSSOP28	96KB Configurable		256B + 3KB	25
DC6688FL96TT-16M-TR1	TSSOP28[1]	96KB Configurable		256B + 3KB	25

[1] Tape and reel packing.

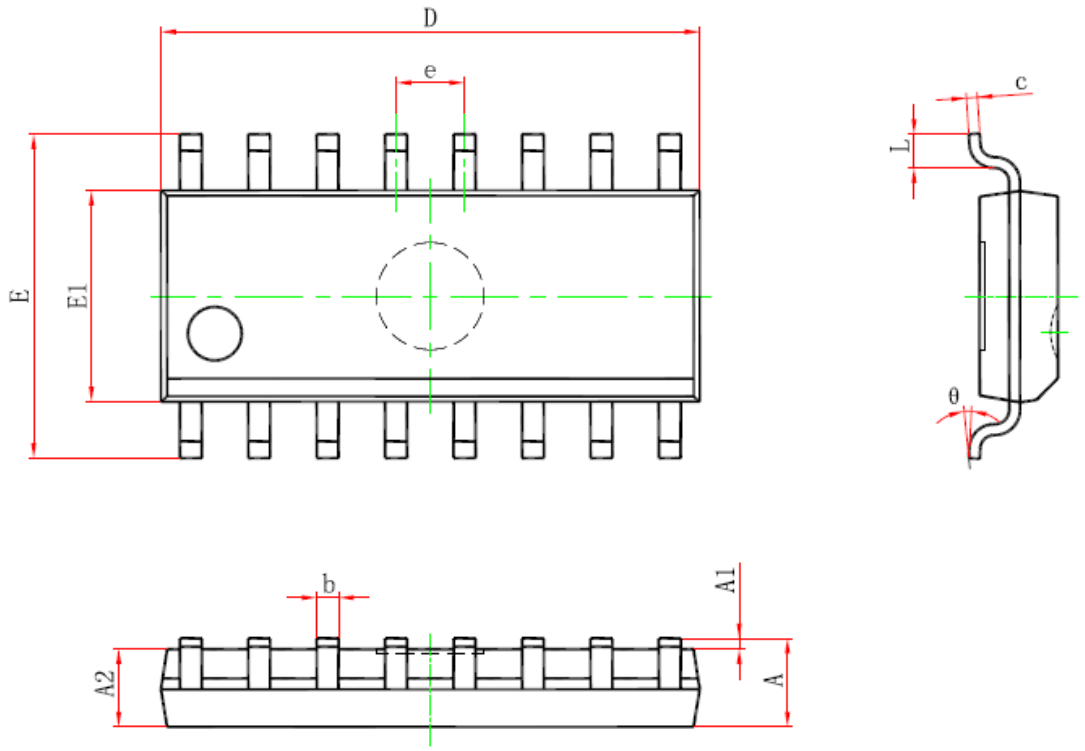
17 Package Outlines

17.1 8-pin TSSOP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

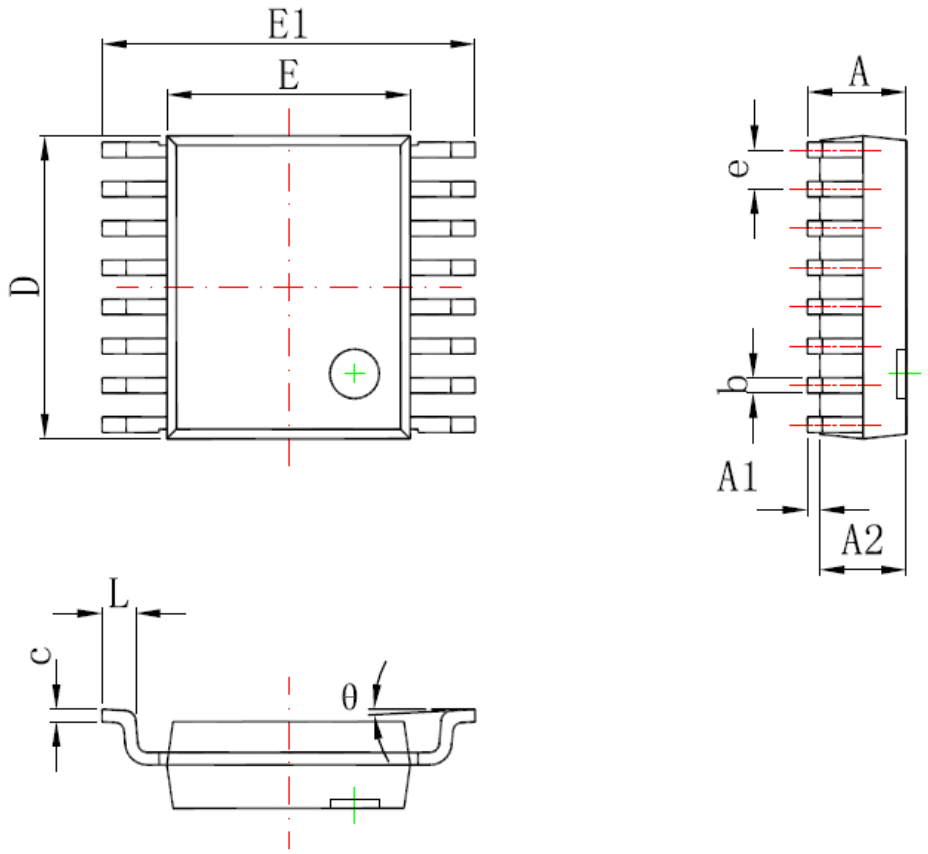
17.2 16-pin SOP



NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AC DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

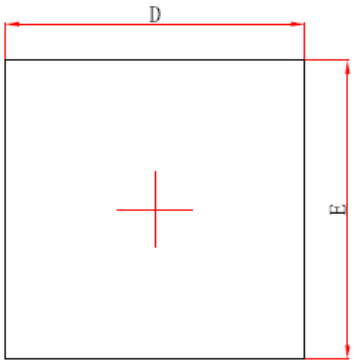
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	---	1.750	---	0.069
A1	0.100	0.250	0.004	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

17.3 16-pin SSOP

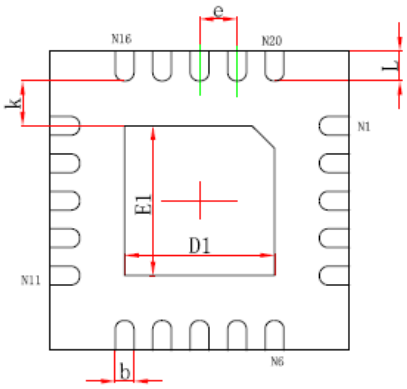


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

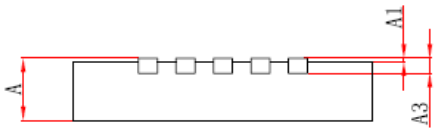
17.4 20-pin QFN



Top View



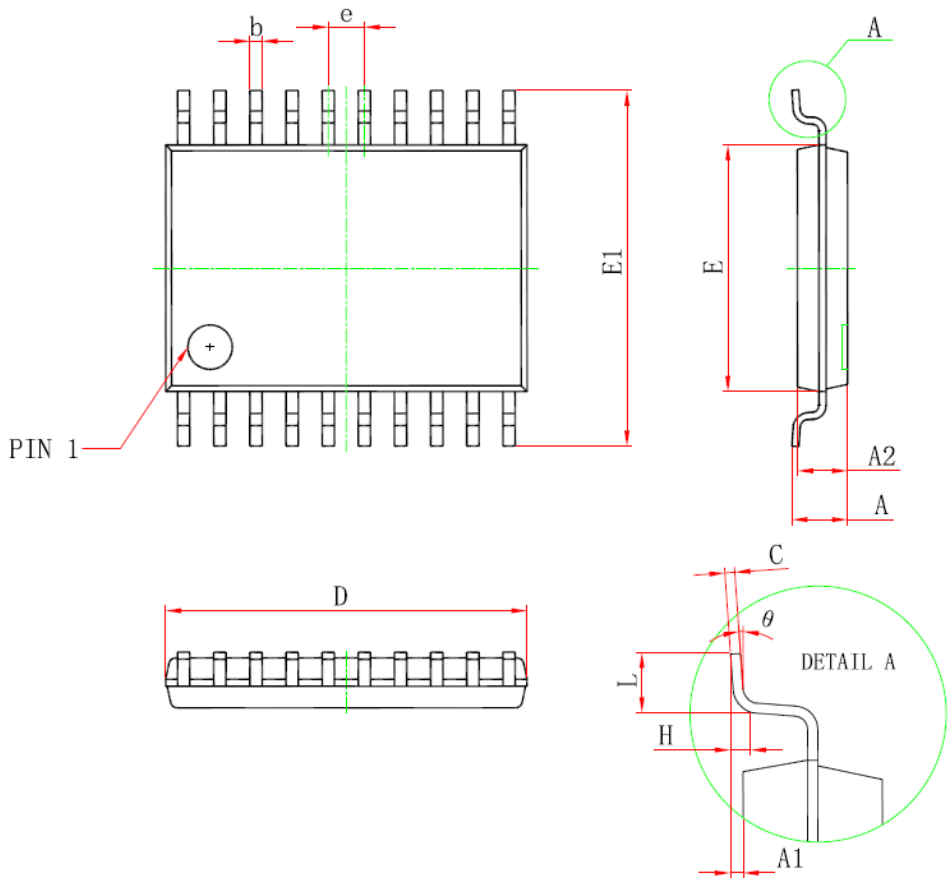
Bottom View



Side View

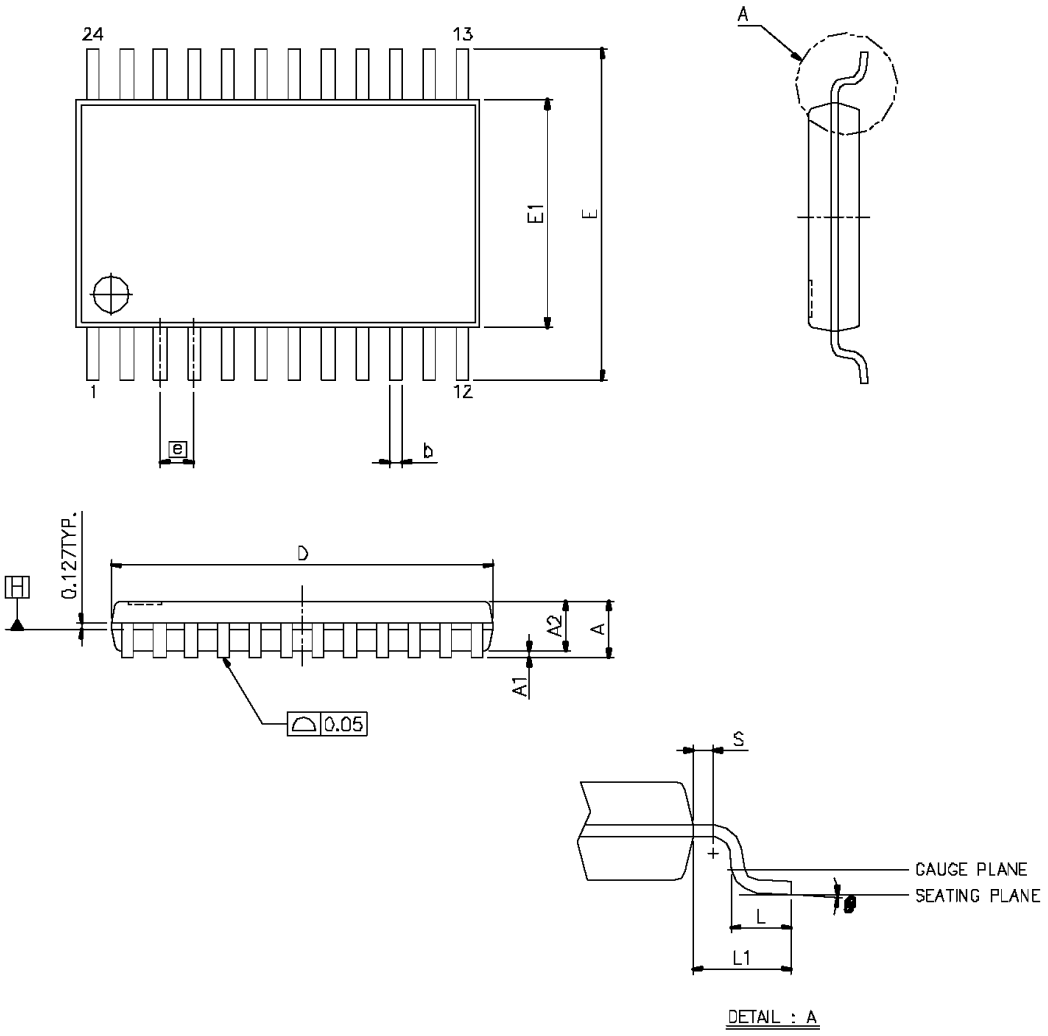
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	1.900	2.100	0.075	0.083
E1	1.900	2.100	0.075	0.083
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

17.5 20-pin TSSOP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

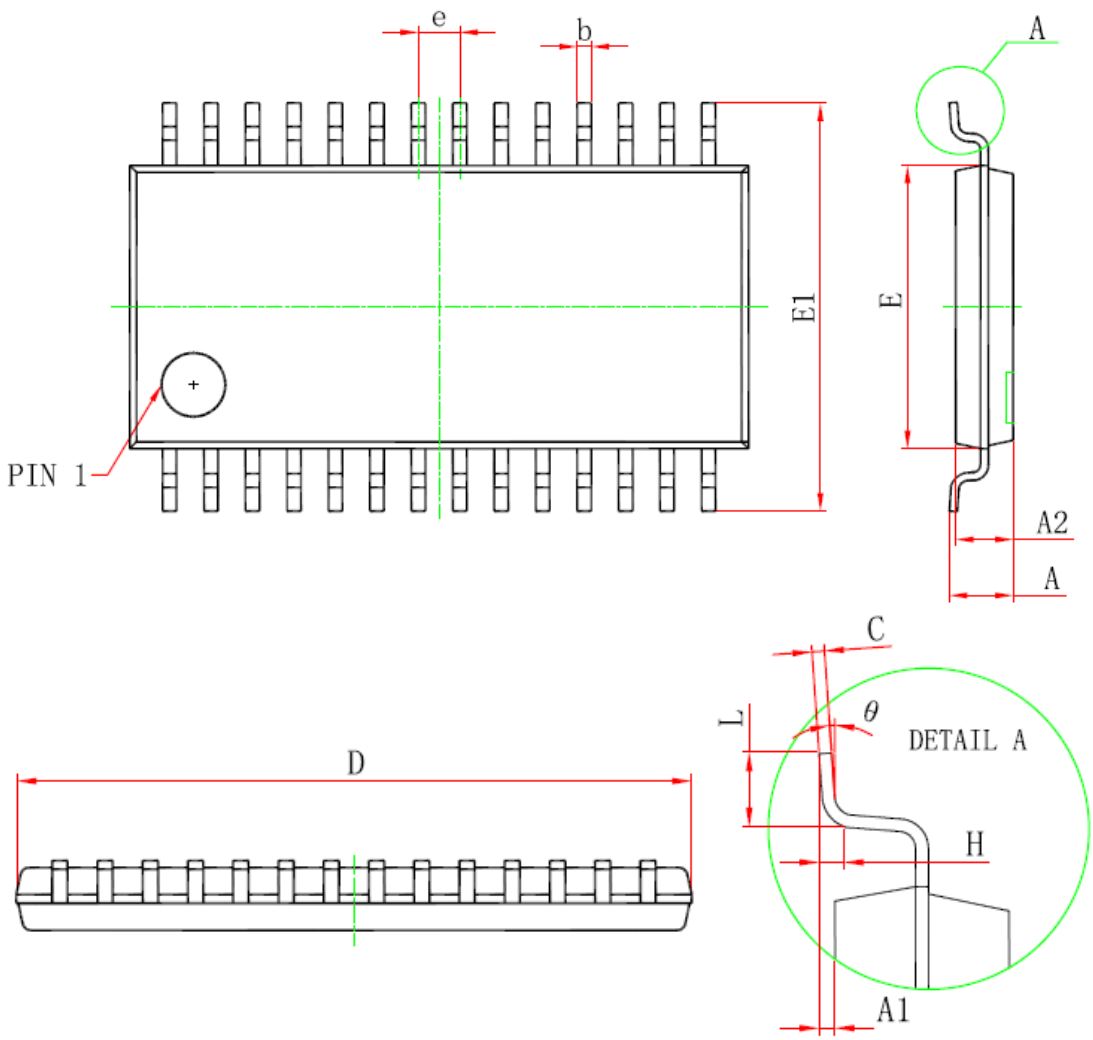
17.6 24-pin TSSOP



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Dimensions in millimeters

17.7 28-pin TSSOP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

18 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	25 Jun, 2013	All	-	New template	Anthony Chong	Danny Ho, Kennis To
1.1	10 Jul, 2013	All	-	Correct the format	Kennis To	Anthony Chong
1.2	26 Jul, 2013	4.2	9	Correct the memory address	Kennis To	Celia Ki
1.3	22 Aug, 2013	All	-	Add DC6688FL16T/32T	Anthony Chong	Danny Ho Patrick Li
1.4	15 Oct, 2013	4 1.8	-	Revise register description Revise oscillator spec	Celia Ki	Anthony Chong
1.5	31 Oct, 2013	1.2 1.8 17.1	-	Add IR transistor spec Add internal oscillator spec Add WLP16 package outline	Celia Ki	Anthony Chong
1.6	28 Nov, 2013	2 17.2	-	Add SOP16 pin assignment Revise ordering information	Anthony Chong	Celia Ki
1.7	4 Feb, 2014	2 8	-	Change from SOP8 to SOP16 Revise the I/O information	Philip Hung	Danny Ho
1.8	24 Mar, 2014	17.1		Update WLP16 information Update the running mode current	Philip Hung	Fred Law
1.9	24 Mar, 2014	1		Update the running mode current	Philip Hung	Fred Law
2.0	28 Apr, 2014	All	-	Remove SOP16 information	Danny Ho	Philip Hung
2.1	9 Jun, 2014	All	-	Remove WLP16 information Add pull down resistance	Kennis To	Danny Ho
2.2	28 Jul, 2014	All		Add 20-pin TSSOP	Kennis To	Eddy Cheung
2.3	31 Jul, 2014	All		Revise DC6688FL64/96T	Kennis To	Danny Ho
2.4	14 Aug, 2014	All		Revise 20-pin TSSOP assignment	Kennis To	Danny Ho
2.5	30 Nov, 2014	2, 17		Add SOP16 information	Danny Ho	Patrick Li
2.6	15 Mar, 2016	2, 17		Add SSOP16 information	Danny Ho	Patrick Li
2.7	29 Mar, 2016	1.7, 2		Revise 20-pin TSSOP pin function Revise 50kosc spec	Kennis To	Patrick Li
2.8	5 Aug, 2016	16		Add 16MHz internal oscillator	Kennis To	Eddy Cheung
2.9	18 Oct, 2016	All		Add DC6688FL16TQ, DC6688FL32TQ, DC6688FL96TQ, DC6688FL96TH	Kennis To	Eddy Cheung
3.0	31 Oct, 2016	16		Add DC6688FL32T-COB and DC6688FL96T-COB	Kennis To	Eddy Cheung
3.1	21 Aug, 2017	4.2 16 2		Revise address Remove DC6688FL16TQ, DC6688FL32TH, DC6688FL32TT, DC6688FL96TQ Revise QFN20, TSSOP20 pin assignment	Kennis To	Danny Ho
3.2	5 Sept, 2017	All		Add DC6688FL32TR, DC6688FL96TR	Kennis To	Danny Ho
3.3	18 Sept, 2017	All		Add DC6688FL32TY	Kennis To	Danny Ho
3.4	17 Oct, 2017	2, 16		Add T&R option for DC6688FL32TY Add DC6688FL96TQ	Kennis To	Danny Ho
3.5	29 Jun, 2018	16		Add DC6688FL32TH, DC6688FL64TH	Kennis To	Eddy Cheung

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