DC6688FSE

8-Bit 8051 Microcontroller

DC6688FSE is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- Enhanced 8051 8-bit CPU core, MCS51 instructions compatible
- Power Down and Backup modes
- Power Monitor for low battery indicator
- Memory
  - 4KB/8KB/16KB/30KB/62KB Program Flash Memory
  - 64B Data Flash Memory
  - Security bit for read back protection
  - Internal 256B SRAM; Expanded 512B/2KB SRAM
- IR generator by counter A with auto-reload function
- Two-level priority interrupt controller
- 27 bit-programmable I/O ports
- 16-bit Timers x 3
- Standard UART x 2
- SPI Master
- I2C Master
- Low Voltage Detection (LVD) for backup mode
- Low Voltage Indication (LVI)
- Maximum operating voltage: 3.6V
- Operating temperature: -25°C to +85°C
- Package type:
  - 8-pin TSSOP
  - 24-pin TSSOP
  - 28-pin TSSOP
  - 32-pin LQFP

Quick look on Ordering Information

Table of Contents

1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to VDD + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B,C and D[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B,C and D[4]	+100	mA
Operating Temperature	T_A	-	-25 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:
[1] It is measured for any one of I/O pin when configured to push-pull output high.
[2] It is measured as total for Ports A, B, C and D when configured to push-pull output high.
[3] It is measured for any one of I/O pin when configured to push-pull output low.
[4] It is measured as total for Ports A, B, C and D when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH1}	All input pins except XIN	0.7 V_{DD}	-	V_{DD}	V
	V_{IH2}	XIN	V_{DD} – 0.3	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input pins except XIN	0	-	0.3 V_{DD}	V
	V_{IL2}	XIN	0	-	0.3	V
Output High Voltage	V_{OH1}	Port C1, V_{DD} = 2.4V, I_{OH} = - 6mA, T_A = 25°C	V_{DD} – 0.7	-	-	V
	V_{OH2}	Port A, V_{DD} = 2.4V, I_{OH} = - 1mA, T_A = 25°C	V_{DD} – 0.7	-	-	V
	V_{OH3}	All output pins except Port A and Port C1 pins, V_{DD} = 2.4V, I_{OH} = - 2.2mA, T_A = 25°C	V_{DD} – 1.0	-	-	V
Output Low Voltage	V_{OL1}	Port C1, V_{DD} = 2.4V, I_{OL} = 12mA, T_A = 25°C	-	0.4	1	V
	V_{OL2}	Port A, V_{DD} = 2.4V, I_{OL} = 4mA, T_A = 25°C	-	0.4	1	V
	V_{OL3}	All output pins except Port A and Port C1 pins, V_{DD} = 2.4V, I_{OL} = 8mA, T_A = 25°C	-	0.4	1	V
Input High Leakage Current	I_{LIH1}	All input pins except XIN, XOUT and ISPSEL, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH2}	XIN and XOUT, V_{IN} = V_{DD}	-	-	20	µA
	I_{LIH3}	ISPSEL, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins except XIN and XOUT, V_{IN} = 0	-	-	-1	µA
	I_{LIL2}	XIN and XOUT, V_{IN} = 0	-	-	-20	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High Leakage Current	I_{LOH}	All output pins, $V_{OUT} = V_{DD}$	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, $V_{OUT} = 0V$	-	-	-1	µA
Pull-up Resistors (Port A, B and C)	R_{L1}	$V_{DD} = 2.4V$, $V_{IN} = 0$ V; $T_A = 25°C$	20	40	60	kΩ
Supply Current						
Run Mode[1]	Idd(op)	$f_{OSC} = 8MHz$, $V_{DD} = 3.0V$, $T_A = 25°C$	-	2	8	mA
Power Down Mode[2] 62KB 4KB/8KB/16KB/30KB	Idd(pd)	$V_{DD} = 3.0V$, $T_A = 25°C$	 - -	 2 2	 8 5	 µA µA

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is tested if the condition is that:

a) Port A output open-drain.

b) Port B and C input enable pull-up resistor.

c) Port C1 output push-pull.

d) Port D output push-pull.

1.3 Low Voltage Detect circuit Characteristics

(T_A = -25°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}		1.9	2.15	2.3	V
Low Voltage Detect Level	V_{LVD1}		1.5	1.75	2.0	V

Remarks:

[1] $V_{LVD2} - V_{LVD1} = \Delta V$

1.4 SRAM Data Retention Voltage in Power Down Mode

(T_A = -25°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 1.0V Power Down Mode	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -25°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}				
Output Capacitance	C_{OUT}		-	-	10	pF
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

(V_{DD} = 2.5V, T_A = 25°C)

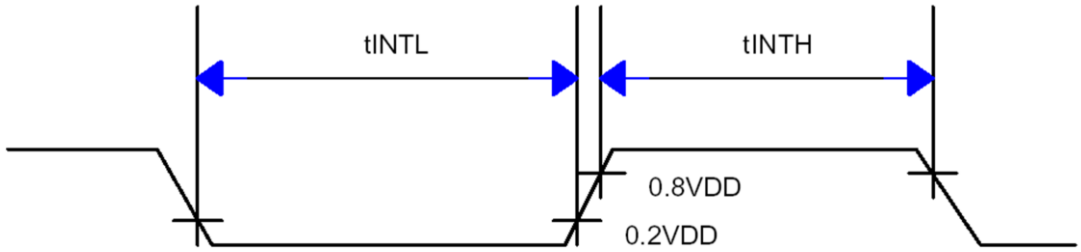
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.7 A.C. Electrical Characteristics

(T_A = -25°C to +85°C)

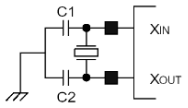
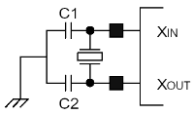
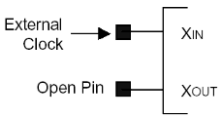
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High, Low width for Port A, B	t_{INTH}, t_{INTL}	PA0 – PA7, PB0 – PB7, V_{DD} = 3.0V	0	-	-	-



Input Timing for Port A, B interrupts

1.8 Oscillation Characteristics

(T_A = -25°C to +85°C)

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	-	12.5	MHz
Ceramic		CPU clock oscillation frequency	1	-	12.5	MHz
External Clock		X_{IN} input frequency	1	-	12.5	MHz

(T_A = -25°C to +85°C, V_{DD} = 3.0V)

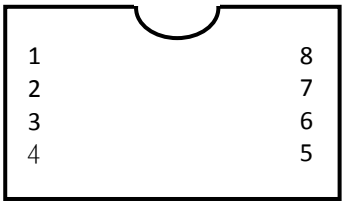
Parameter	Conditions	Min	Typ	Max	Unit
Crystal	f_{OSC} > 1MHz Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range	-	-	20	ms
Ceramic		-	-	10	ms
External Clock	X_{IN} input High and Low width(t_{XL}, t_{XH})	25	-	500	ns
Oscillator Stabilization Wait Time	tWAIT when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
	tWAIT when released by an external interrupt[2]	-	$2^{13}/f_{OSC}$	-	ms

Remarks:

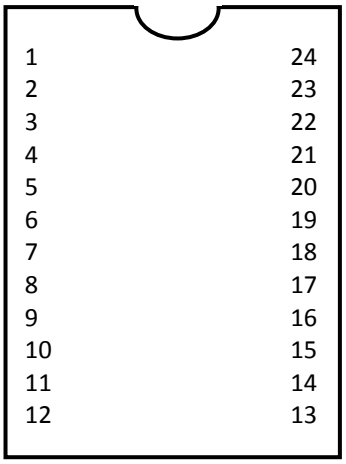
[1] f_{osc} is the oscillator frequency.
[2] The duration of the oscillation stabilization time(tWAIT) when it is released from power down mode by PA or PB interrupt.

2 Pin Assignment

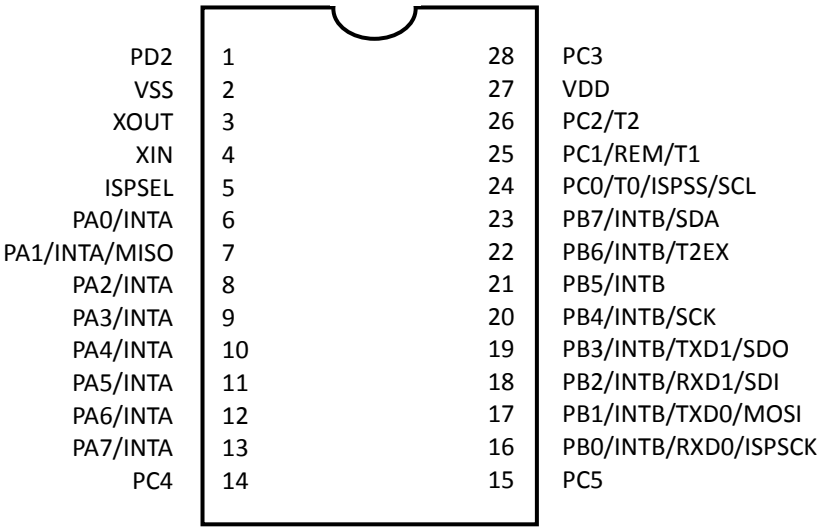
(TSSOP8)



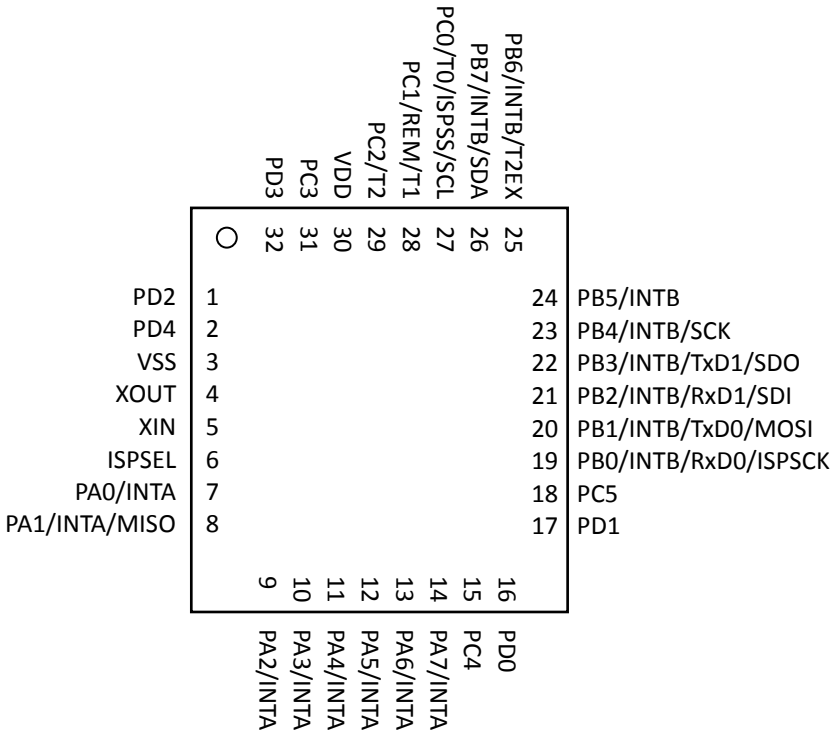
(TSSOP24)



(TSSOP28)



(LQFP32)



TSSOP8	TSSOP24	TSSOP28	LQFP32	Pin Name	Symbol	Function
5	4	5	6	ISPSEL	ISPSEL	SL (Single Line) Communication Signal
3	2	3	4	XOUT	XOUT	Crystal / Oscillator Output
4	3	4	5	XIN	XIN	Crystal / Oscillator Input
1	24	27	30	VDD	VDD	Power
2	1	2	3	VSS	VSS	Ground
-	5	6	7	PA0/INTA	PA0	Configurable input or output port
					INTA	Port Interrupt Input
-	6	7	8	PA1/INTA/MISO	PA1	Configurable input or output port
					INTA	Port Interrupt Input
					MISO	ISP Master In Slave Out
-	7	8	9	PA2/INTA	PA2	Configurable input or output port
					INTA	Port Interrupt Input
-	8	9	10	PA3/INTA	PA3	Configurable input or output port
					INTA	Port Interrupt Input
-	9	10	11	PA4/INTA	PA4	Configurable input or output port
					INTA	Port Interrupt Input
-	10	11	12	PA5/INTA	PA5	Configurable input or output port
					INTA	Port Interrupt Input
-	11	12	13	PA6/INTA	PA6	Configurable input or output port
					INTA	Port Interrupt Input
-	12	13	14	PA7/INTA	PA7	Configurable input or output port
					INTA	Port Interrupt Input
6	13	16	19	PB0/INTB/RxD0/ISPSCK	PB0	Configurable input or output port
					INTB	Port Interrupt Input
					RxD0	UART receiver data input

TSSOP8	TSSOP24	TSSOP28	LQFP32	Pin Name	Symbol	Function
					ISPSCK	ISP Serial clock
7	14	17	20	PB1/INTB/TxD0/MOSI	PB1	Configurable input or output port
					INTB	Port Interrupt Input
					TxD0	UART transmitter data output
					MOSI	ISP Master Out Slave In
-	15	18	21	PB2/INTB/RxD1/SDI	PB2	Configurable input or output port
					INTB	Port Interrupt Input
					RxD1	UART receiver data input
					SDI	SPI Serial Data In
-	16	19	22	PB3/INTB/TxD1/SDO	PB3	Configurable input or output port
					INTB	Port Interrupt Input
					TxD1	UART transmitter data output
					SDO	SPI Serial Data Out
-	17	20	23	PB4/INTB/SCK	PB4	Configurable input or output port
					INTB	Port Interrupt Input
					SCK	SPI Serial Clock
-	18	21	24	PB5/INTB	PB5	Configurable input or output port
					INTB	Port Interrupt Input
-	19	22	25	PB6/INTB/T2EX	PB6	Configurable input or output port
					INTB	Port Interrupt Input
					T2EX	Timer 2 Capture-reload trigger / up down count
-	20	23	26	PB7/INTB/SDA	PB7	Configurable input or output port
					INTB	Port Interrupt Input
					SDA	I2C Serial Data
-	21	24	27	PC0/T0/ISPSS/SCL	PC0	High current drive configurable I/0
					T0	Timer 0 External counter Input
					ISPSS	ISP Slave Select
					SCL	I2C Serial Clock
8	22	25	28	PC1/REM/T1	PC1	High current drive configurable I/0
					REM	Counter A Carrier Frequency Output
					T1	Timer 1 External Counter Input
-	23	26	29	PC2/T2	PC2	High current drive configurable I/0
					T2	Timer 2 External Counter Input
-	-	28	31	PC3	PC3	High current drive configurable I/0
-	-	14	15	PC4	PC4	High current drive configurable I/0
-	-	15	18	PC5	PC5	High current drive configurable I/0
-	-	-	16	PD0	PD0	High current drive configurable I/0
-	-	-	17	PD1	PD1	High current drive configurable I/0
-	-	1	1	PD2	PD2	High current drive configurable I/0
-	-	-	32	PD3	PD3	High current drive configurable I/0
-	-	-	2	PD4	PD4	High current drive configurable I/0

3 Description

DC6688FSE is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with enhanced 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) for IR remote controller application. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

4 Memory

Memory comprises of the following elements, namely:

- 4KB/8KB/16KB/30KB/62KB Program Flash memory
- 64B Data Flash memory
- 256B Internal SRAM
- 512B/2KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

4.1 Program & Data Flash Memory

On-chip program Flash size range from 4096 bytes to 63488 bytes, and a 64 bytes data Flash are provided for selection upon different application. It can be programmed by In-System-Programming (ISP) method.

In addition, write protection signature is available to avoid writing accidentally.

4.2 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, UART, etc. Some locations in the SFR address space are addressable as bits.

4.3 External Function Register (XFR)

The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

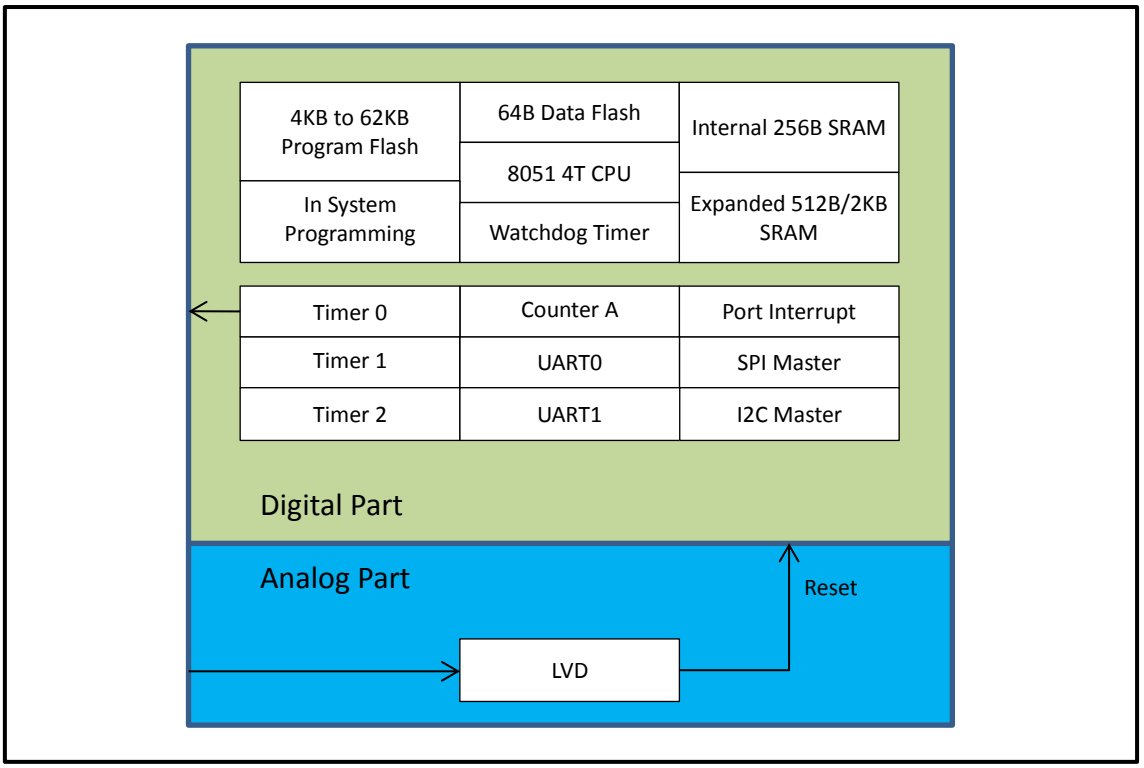
5 Architecture

With the 4T 8051 8-bit CPU, instruction execution time is 500ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a

simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

The block diagram is illustrated in the following figure.



6 Central Processing Unit (CPU)

The 4T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

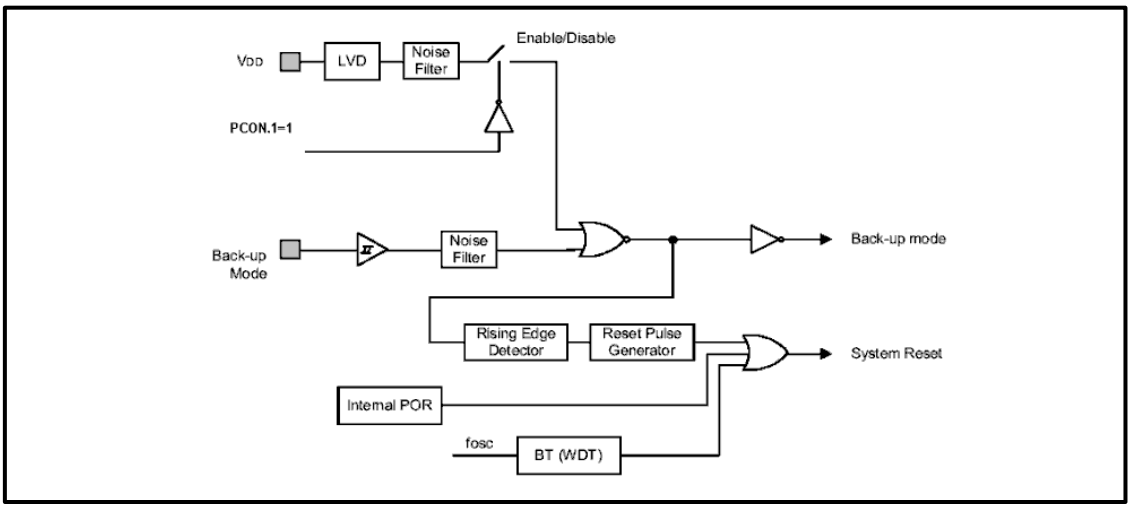
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

7 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



8 I/O port

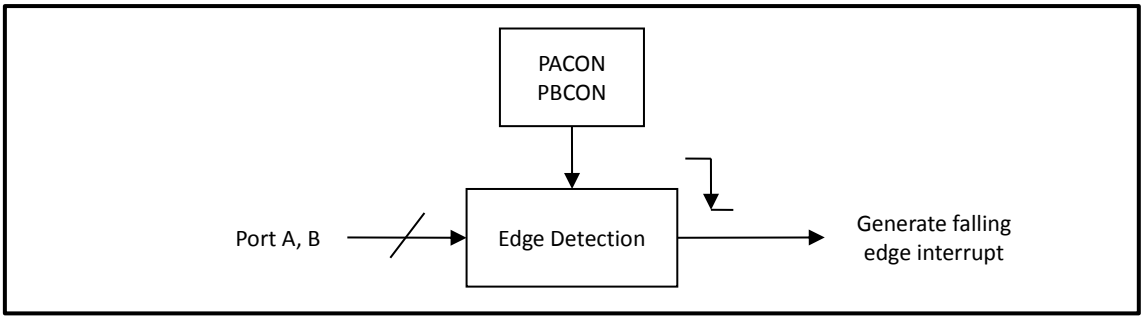
The 8-pin package has two 2-bit ports (PB) and one 1-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines. On reset, Port B is set to the value (11111111). Port C is set to the value (00111101).

The 24-pin package has two 8-bit ports (PA and PB) and one 3-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (11111111). Port C is set to the value (00111101).

The 28-pin package has two 8-bit ports (PA and PB), one 6-bit port (PORTC) and one 1-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (11111111), Port C is (00111101) and Port D is (00011111).

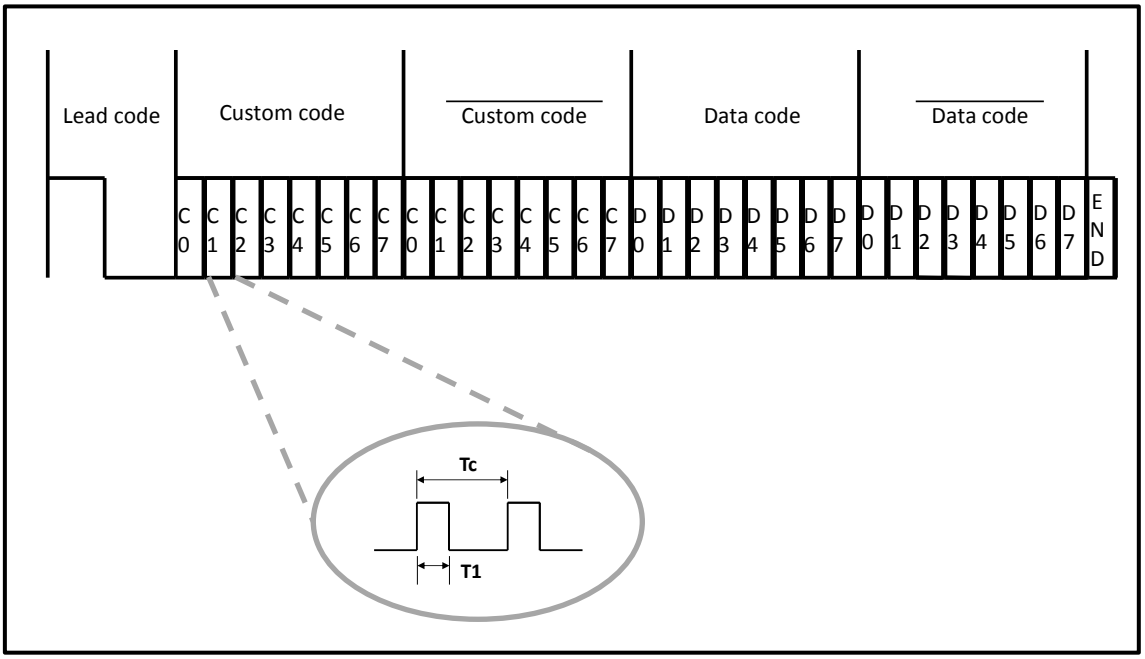
The 32-pin package has two 8-bit ports (PA and PB), one 6-bit port (PORTC), and one 5-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (11111111), Port C is (00111101), and Port D is (00011111).

Port interrupt function is supported for port A and B. Pull-up resistors are also included in port A and B and could be assigned pin-by-pin by programming the pull-up resistor enable register. Port C and D can be configured individually to input mode, open-drain output mode, or push-pull output mode.



9 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



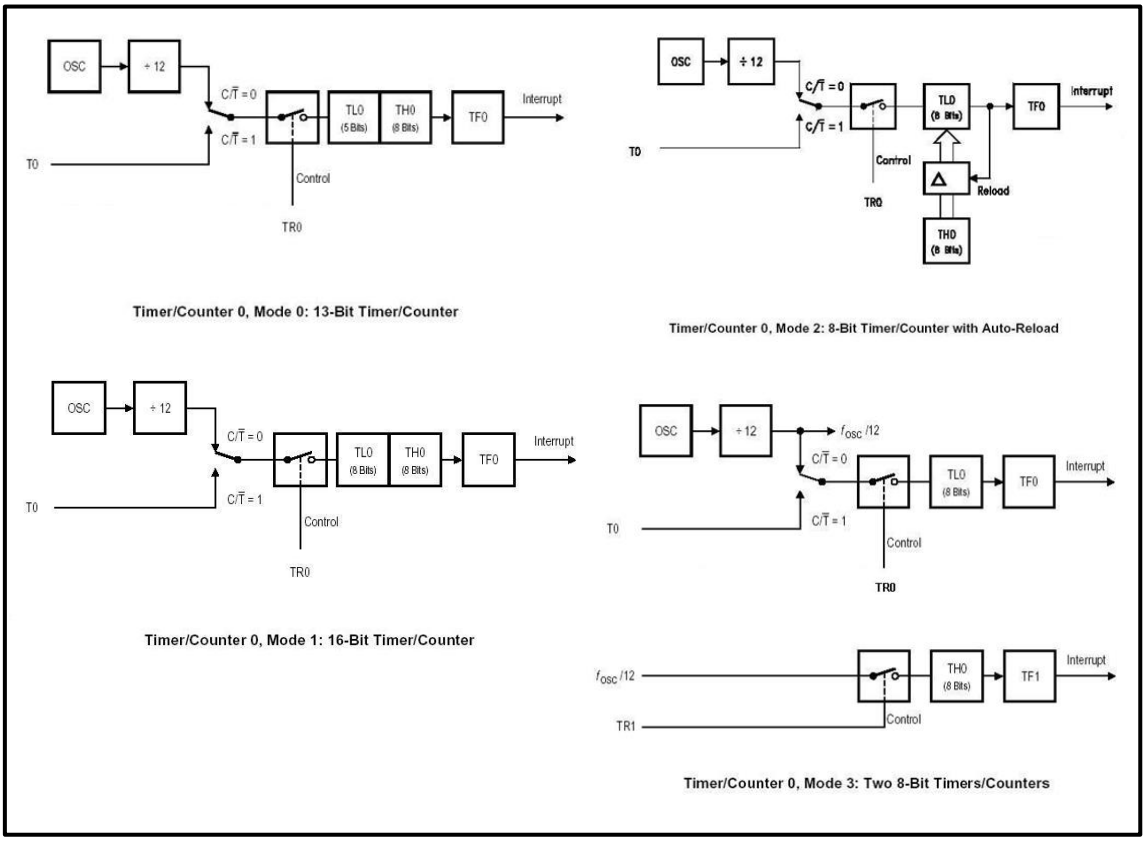
Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

10 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



11 Enhanced UART

The UART operates in all of the usual modes and perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

The full duplex UART ports are able to transmit and receive simultaneously. These serial ports are also receive-buffered. It can commence reception of a second byte before the previously received byte has been read from the receive register. If, however, the first byte has still not been read by the time reception of the second byte is complete, one of the bytes will be lost. The SIO receive and transmit registers are both accessed via the SBUF special function register. Writing to SBUF loads the transmit register, and reading SBUF accesses to a physically separate receive register. SIO can operate in 4 modes.

The UART operates in four modes (one synchronous and three asynchronous). The Serial 0 is buffered at the receive side, i.e. it can receive new data while the previously received is not damaged in the receive register until the completion of the 2nd transfer.

The UART is fully compatible with the standard 8051 serial channel.

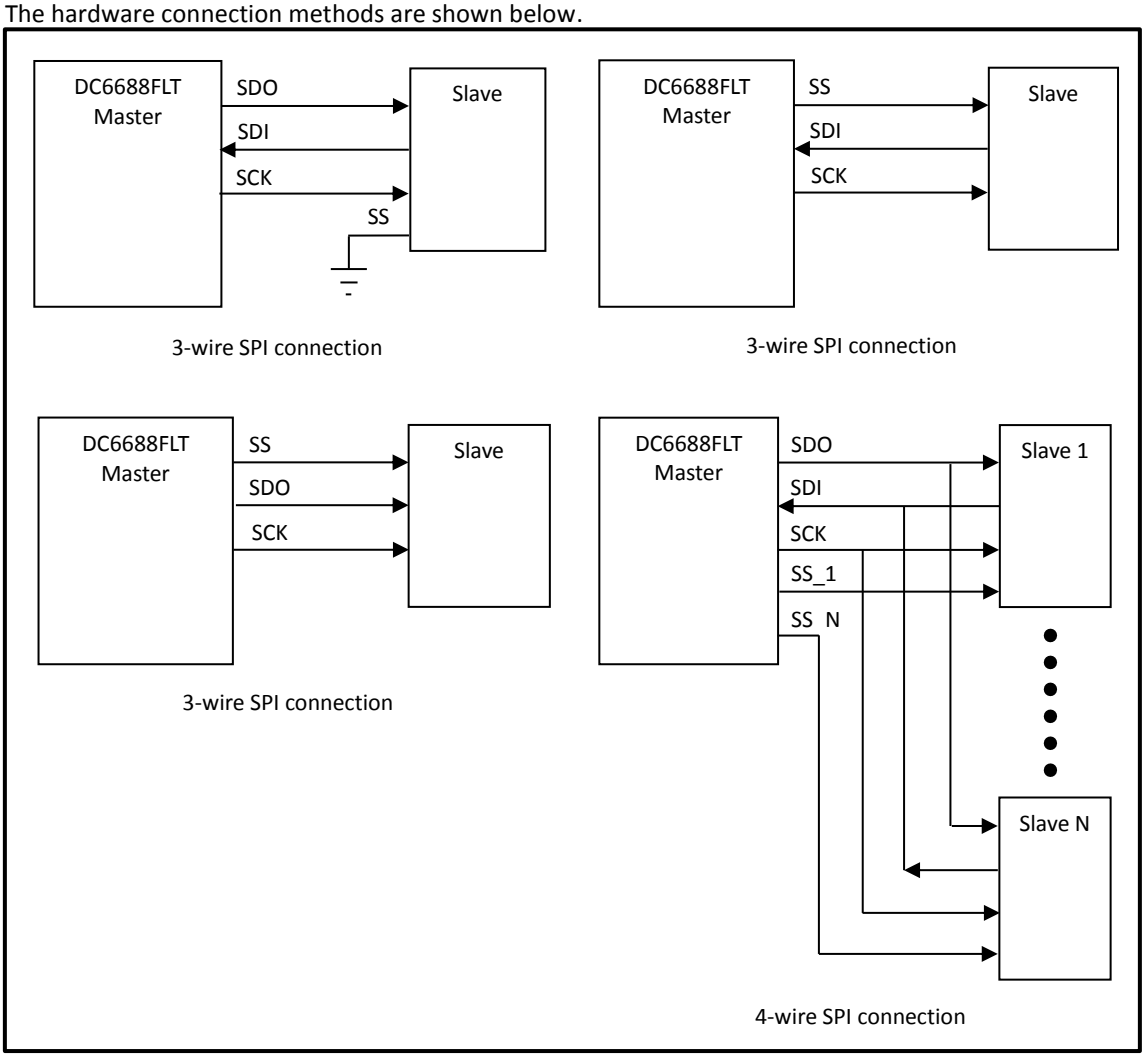
12 Serial Peripheral Interface

A complete hardware Serial Peripheral Interface (SPI) on-chip in master mode is integrated. SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously.

The SPI interface consists of the following wires:

- SDI
  The SDI line on the master (data in) should be connected to the SDO/MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.
- SDO
  The SDO line on the master (data out) should be connected to the SDI/MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.
- SCK
  The master serial clock (SCK) is used to synchronize the data being transmitted and received through the SDO and SDI data lines. A single data bit is transmitted and received in each SCK period. Therefore, a byte is transmitted/received after eight SCK periods.
- SS
  In the slave device, SPI interface requires the slave select line (SS) to enable communication such that DC6688FLT (master) can talk to more than one slave device in different time slot. To be able to talk to the slave device, master should assert the SS pin on an external slave device. This can be done by using a Port digital output pin which is manually controlled by software.

The hardware connection methods are shown below.



13 Inter-Integrated Circuit (I2C) Interface

The I2C Bus Controller supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: “SCL” (serial clock line) and “SDA” (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus.

The interface defines 2 transmission speeds if 12MHz crystal is used:
- Normal: 100Kbps
- Fast: 400Kbps

The I2C component performs 8-bit-oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode and may operate in the two modes.

Mode	Description
Master Transmitter Mode	Serial data output through SDA while SCL output the serial clock.
Master Receiver Mode	Serial data is received via SDA while SCL outputs the serial clock.

14 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires only 3 wires to minimize the number of added components and board area impact.

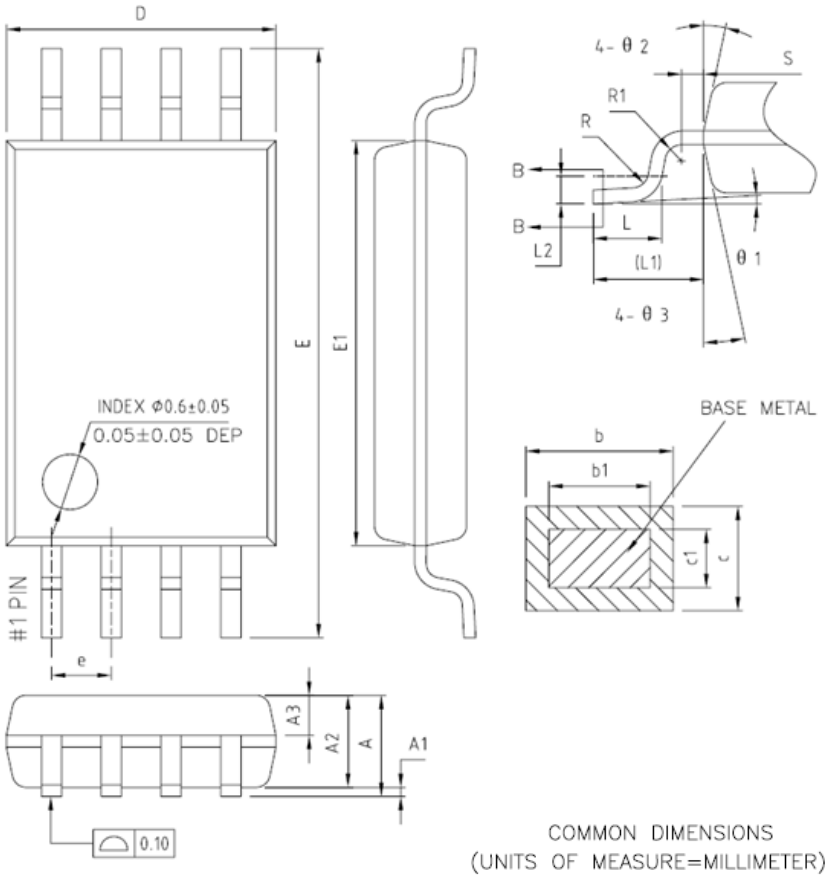
15 Ordering Information

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688F4SEY	TSSOP8	4KB	64B	256B + 512B	3
DC6688F4SEY-TR1	TSSOP8[1]	4KB	64B	256B + 512B	3
DC6688F4SET	TSSOP24	4KB	64B	256B + 512B	19
DC6688F4SET-TR1	TSSOP24[1]	4KB	64B	256B + 512B	19
DC6688F4SEET	TSSOP28	4KB	64B	256B + 512B	23
DC6688F4SEET-TR1	TSSOP28[1]	4KB	64B	256B + 512B	23
DC6688F8SET	TSSOP24	8KB	64B	256B + 512B	19
DC6688F8SET-TR1	TSSOP24[1]	8KB	64B	256B + 512B	19
DC6688F8SEET	TSSOP28	8KB	64B	256B + 512B	23
DC6688F8SEET-TR1	TSSOP28[1]	8KB	64B	256B + 512B	23
DC6688F16SET	TSSOP24	16KB	64B	256B + 512B	19
DC6688F16SEET	TSSOP28	16KB	64B	256B + 512B	23
DC6688F16SEET-TR1	TSSOP28[1]	16KB	64B	256B + 512B	23
DC6688F16SEEE	LQFP32	16KB	64B	256B + 512B	27
DC6688F30SET	TSSOP24	30KB	64B	256B + 512B	19
DC6688F30SEET	TSSOP28	30KB	64B	256B + 512B	23
DC6688F30SEET-TR1	TSSOP28[1]	30KB	64B	256B + 512B	23
DC6688F30SEEE	LQFP32	30KB	64B	256B + 512B	27
DC6688F62SET	TSSOP28	62KB	64B	256B + 2KB	23
DC6688F62SET-TR1	TSSOP28[1]	62KB	64B	256B + 2KB	23
DC6688F62SEE	LQFP32	62KB	64B	256B + 2KB	27

[1] Tape and reel packing.

16 Package Outlines

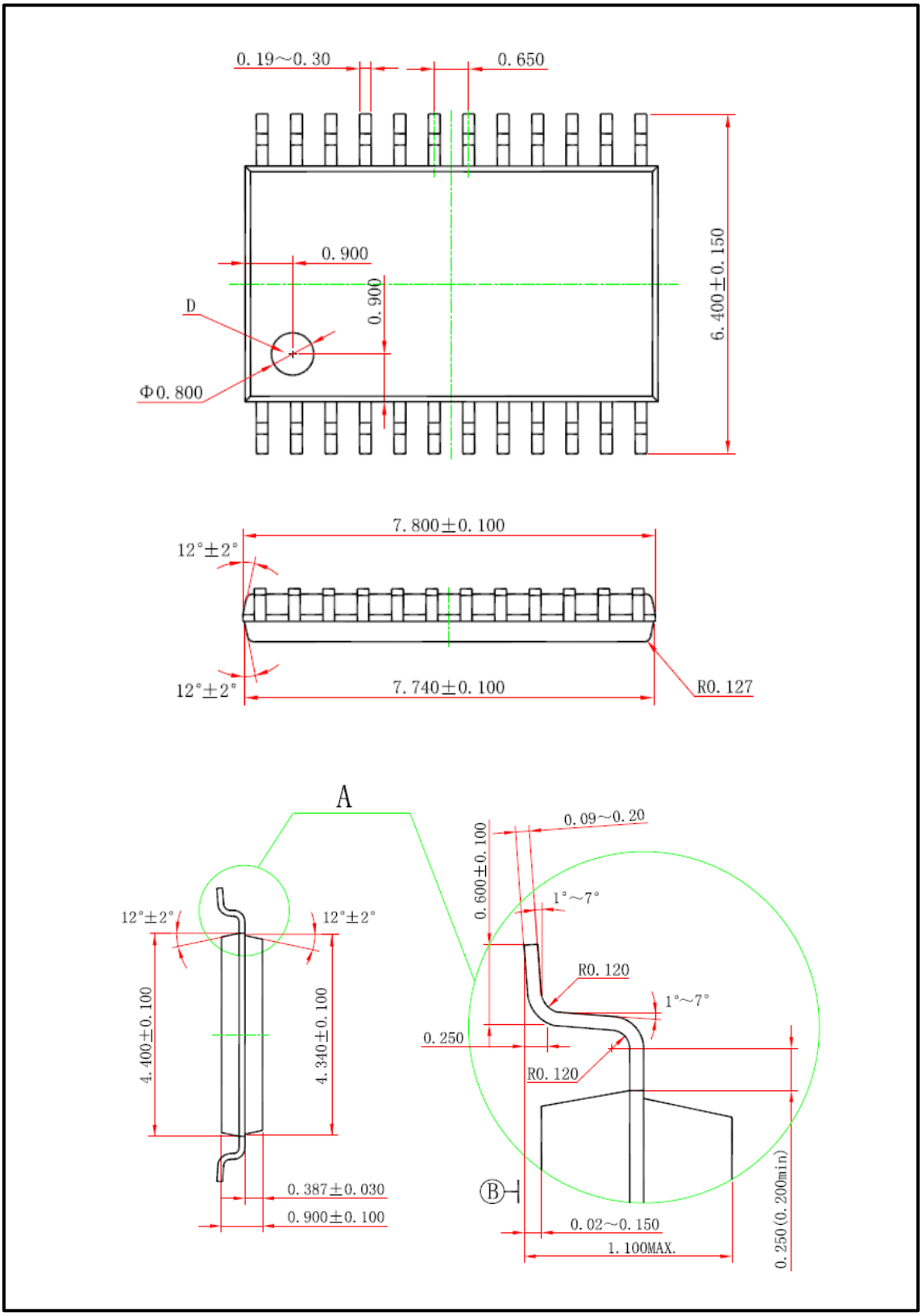
16.1 8-pin TSSOP



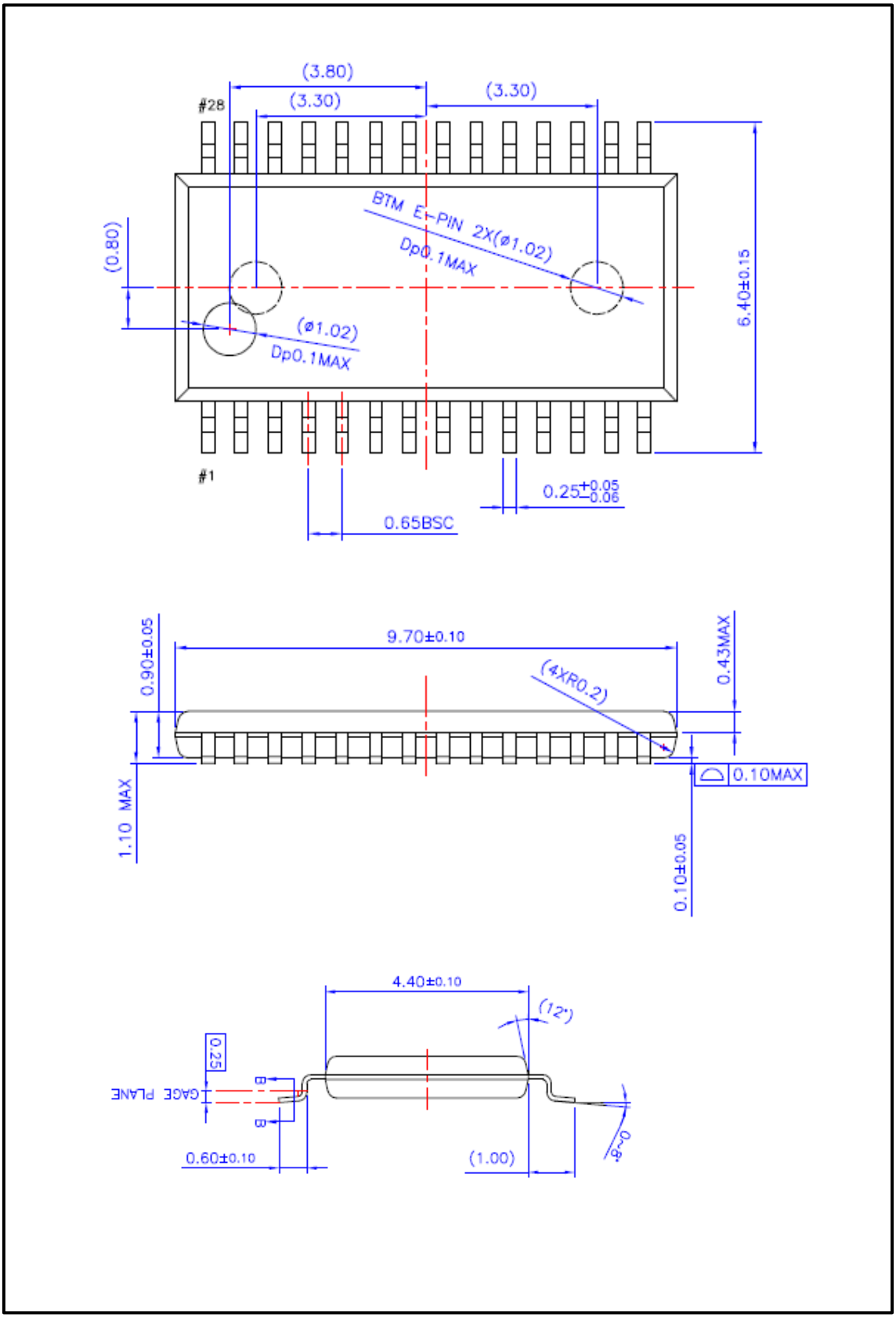
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	2.83	2.93	3.03
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

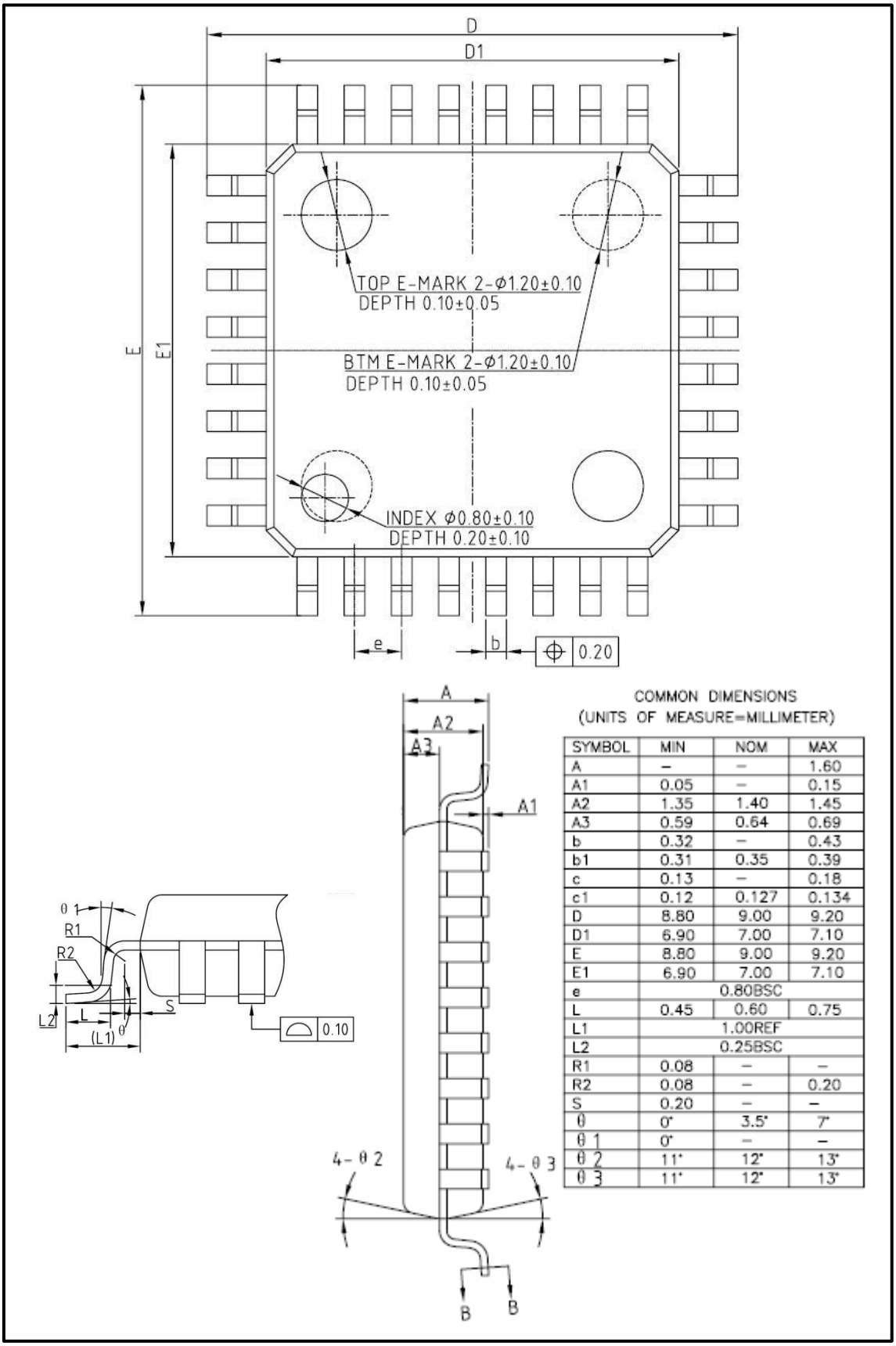
16.2 24-pin TSSOP



16.3 28-pin TSSOP



16.4 32-pin LQFP



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

17 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	26 Jul, 2013	All	-	New template	Kennis To	Celia Ki
1.1	30 Oct, 2013	4	-	Revise register description	Celia Ki	Anthony Chong
1.2	30 Apr, 2014	2, 8, 15, 16	-	Add TSSOP8	Kennis To	Danny Ho
1.3	27 Jul, 2016	1.2	3	Update the wordings	Kennis To	Patrick Li

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