DC6688FST

Super 1T 8051 Microcontroller

DC6688FST is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Power Down and Backup modes
- Memory
  - 4KB/16KB/29.5KB Program Flash Memory
  - 64B Data Flash Memory
  - Security bit for read back protection
  - Internal 256B SRAM; Expanded 1.5KB SRAM
- Internal 12MHz oscillator
  - ± 1% accuracy from -20°C to +70°C, 1.8V to 3.6V
- Built-in transistor for IR LED (I_{OL} = 300mA at V_{OL} = 0.5V)
- IR generator by counter A with auto-reload function
- 4-level priority interrupt controller
- 21 bit-programmable I/O ports
- 16-bit Timers x 3
- 8-bit PWM x 2
- Standard UART
- SPI Master
- I2C Master/Slave
- Low Voltage Detection (LVD) for backup mode
- Low Voltage Indication (LVI) - Programmable
- Maximum operating voltage: 3.6V
- Operating temperature: -40°C to +85°C
- Package type:
  - 20-pin TSSOP
  - 24-pin TSSOP

Quick look on Ordering Information

Table of Contents

1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to VDD + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total current for all I/O pins[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total current for all I/O pins (except Port C1)[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:

[1] It is measured for any one of I/O pin when configured to push-pull output high.

[2] It is measured as total for Ports A, B, C and D when configured to push-pull output high.

[3] It is measured for any one of I/O pin when configured to push-pull output low.

[4] It is measured as total for Ports A, B, C and D when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	All input pins	0	-	0.3 V_{DD}	V
Output High Voltage	V_{OH2}	V_{DD} = 2.4V, I_{OH} = - 2.2mA, T_A = 25°C	V_{DD} - 0.7	-	-	V
Output Low Voltage	V_{OL_IRDRV}	Port C1, IRDRV = 0x3, V_{DD} = 2.4V, I_{OL} = 300mA, T_A = 25°C	-	-	0.5	V
	V_{OL}	All output except Port C1, V_{DD} = 2.4V, I_{OL} = 8mA, T_A = 25°C	-	0.4	1	V
Input High Leakage Current	I_{LIH1}	All input pins except ISPSEL, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH2}	ISPSEL, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins, V_{IN} = 0	-	-	-1	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{L1}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	40	80	160	kΩ
Supply Current Run Mode [1]	Idd(op)	f_{OSC} = 12MHz, V_{DD} = 3.0V, T_A = 25°C	-	2	8	mA
Supply Current Stop Mode[2]	Idd(pd)	V_{DD} = 3.0V, T_A = 25°C	-	2	5	uA

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is measured under the following conditions (Port A: Open-drain mode output Low; Port B and C (except Port C1): Input mode with pull-up resistors enabled; Port C1: Push-pull output mode high; Port D: Push-pull mode output high).

1.3 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Program setting	1.65	1.8	1.95	V
		Default setting	2.0	2.15	2.3	V
		Program setting	2.35	2.5	2.65	V
		Program setting	2.65	2.8	2.95	V
Low Voltage Detect Level	V_{LVD1}		1.5	1.6	1.7	V

Remarks:
[1] $V_{LVD2} - V_{LVD1} = \Delta V$

1.4 SRAM Data Retention Voltage

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Current	I_{DDDR}	V_{DDDR} = 1.0V, Stop mode	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.7 Oscillation Characteristics

Oscillator	Conditions	Min	Typ	Max	Unit
Internal 12MHz Oscillator	T_A = -20°C to +70°C, V_{DD} = 1.8V to 3.6V	-	-	± 1%	MHz

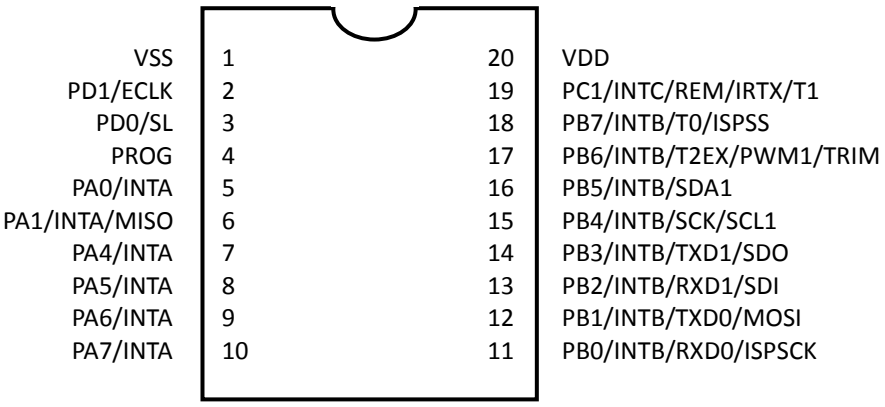
(T_A = -40°C to +85°C, V_{DD} = 3.0V)

Parameter	Conditions	Min	Typ	Max	Unit
Oscillator Stabilization Wait Time	t_{WAIT} when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
	t_{WAIT} when released from Stop mode[2]	-	$2^{13}/f_{OSC}$	-	ms

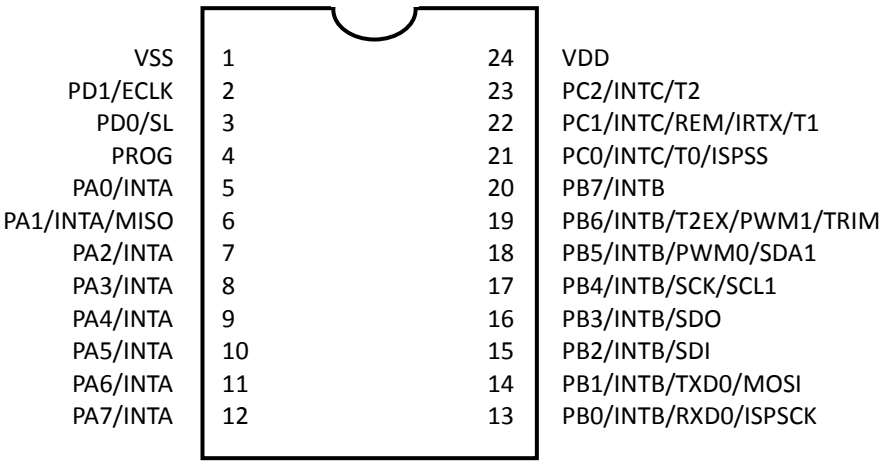
Remarks:
[1] f_{osc} is the oscillator frequency.
[2] Stop mode released by port interrupt.

2 Pin Assignment

(TSSOP20)



(TSSOP24)



TSSOP20	TSSOP24	Pin Name	Symbol	Function
4	4	PROG	PROG	Programming select
20	24	VDD	VDD	Power
1	1	VSS	VSS	Ground
5	5	PA0/INTA	PA0	Configurable input or output port
			INTA	Port Interrupt Input
6	6	PA1/INTA/MISO	PA1	Configurable input or output port
			INTA	Port Interrupt Input
			MISO	ISP Master In Slave Out
-	7	PA2/INTA	PA2	Configurable input or output port
			INTA	Port Interrupt Input
-	8	PA3/INTA	PA3	Configurable input or output port
			INTA	Port Interrupt Input
7	9	PA4/INTA	PA4	Configurable input or output port
			INTA	Port Interrupt Input
8	10	PA5/INTA	PA5	Configurable input or output port
			INTA	Port Interrupt Input
9	11	PA6/INTA	PA6	Configurable input or output port
			INTA	Port Interrupt Input
10	12	PA7/INTA	PA7	Configurable input or output port
			INTA	Port Interrupt Input

TSSOP20	TSSOP24	Pin Name	Symbol	Function
11	13	PB0/INTB/RxD0/ISPSCK	PB0	Configurable input or output port
			INTB	Port Interrupt Input
			RxD0	UART receiver data input
			ISPSCK	ISP Serial clock
12	14	PB1/INTB/TxD0/MOSI	PB1	Configurable input or output port
			INTB	Port Interrupt Input
			TxD0	UART transmitter data output
			MOSI	ISP Master Out Slave In
13	15	PB2/INTB/SDI	PB2	Configurable input or output port
			INTB	Port Interrupt Input
			SDI	SPI Serial Data In
14	16	PB3/INTB/SDO	PB3	Configurable input or output port
			INTB	Port Interrupt Input
			SDO	SPI Serial Data Out
15	17	PB4/INTB/SCK/SCL1	PB4	Configurable input or output port
			INTB	Port Interrupt Input
			SCK	SPI Serial Clock
			SCL1	I2C master/slave serial clock
16	18	PB5/INTB/PWM0/SDA1	PB5	Configurable input or output port
			INTB	Port Interrupt Input
			SDA1	I2C master/slave serial data
17	19	PB6/INTB/T2EX/PWM1/ TRIM	PB6	Configurable input or output port
			INTB	Port Interrupt Input
			T2EX	Timer 2 Capture-reload trigger / up down count
			TRIM	Clock trimming
18	20	PB7/INTB/T0[1]/ISPSS[1]	PB7	Configurable input or output port
			INTB	Port Interrupt Input
			T0[1]	Timer 0 external counter input
			ISPSS[1]	ISP slave select
-	21	PC0/INTC/T0/ISPSS	PC0	Configurable input or output port
			INTC	Port interrupt input
			T0	Timer 0 External counter Input
			ISPSS	ISP Slave Select
19	22	PC1/INTC/REM/T1	PC1	Configurable input or output port
			INTC	Port interrupt input
			REM	Counter A Carrier Frequency Output
			IRTX	IR Transmit with built-in transistor
			T1	Timer 1 External Counter Input
-	23	PC2/INTC/T2	PC2	Configurable input or output port
			INTC	Port interrupt input
			T2	Timer 2 External Counter Input
3	3	PD0/INTD/SL	PD0	Configurable input or output port
			INTD	Port interrupt input
			SL	SL (Single Line) communication signal
2	2	PD1/INTD/ECLK	PD1	Configurable input or output port
			INTD	Port interrupt input
			ECLK	External clock for programming

Remarks:
[1] For TSSOP20 only

3 Description

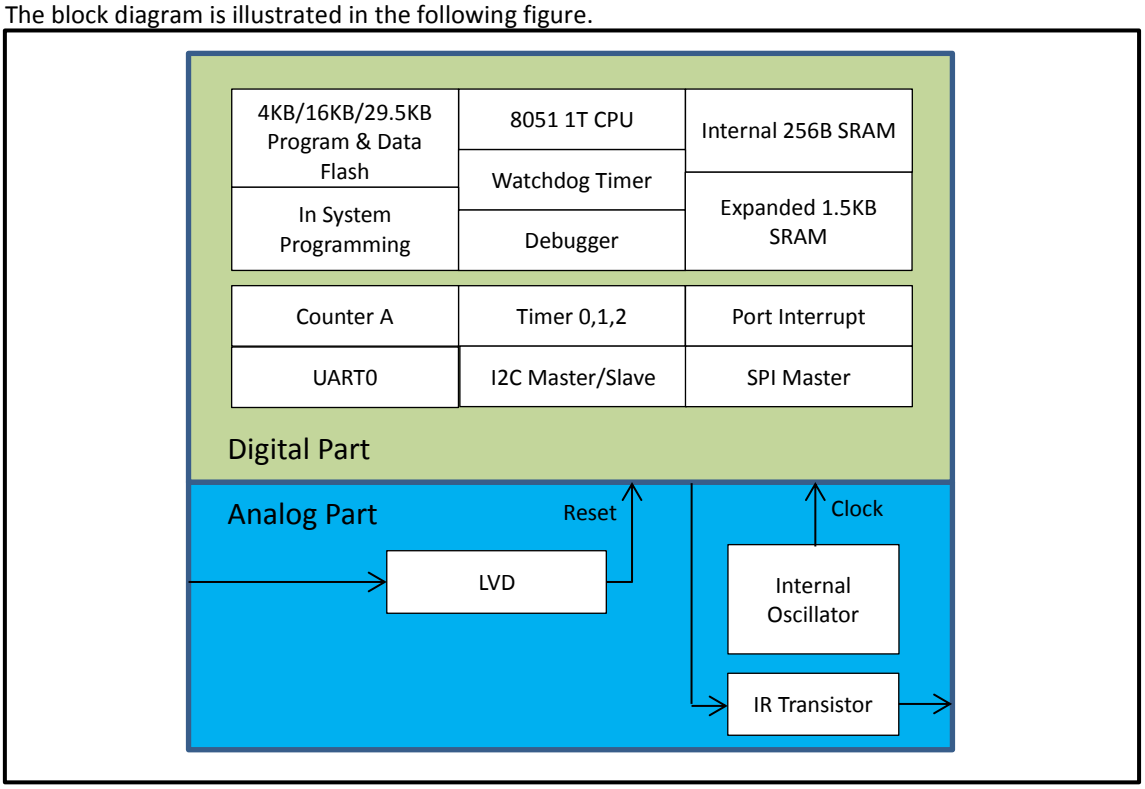
DC6688FST is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory. Internal RC oscillator is equipped, generating 12MHz, 4MHz and 1MHz machine clock without any external components.

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) for IR remote controller application. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

The block diagram is illustrated in the following figure.



4 Memory

Memory comprises of the following elements, namely:

- 4KB/16KB/29.5KB Program Flash memory
- 64B Data Flash memory
- 256B Internal SRAM
- 1.5KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

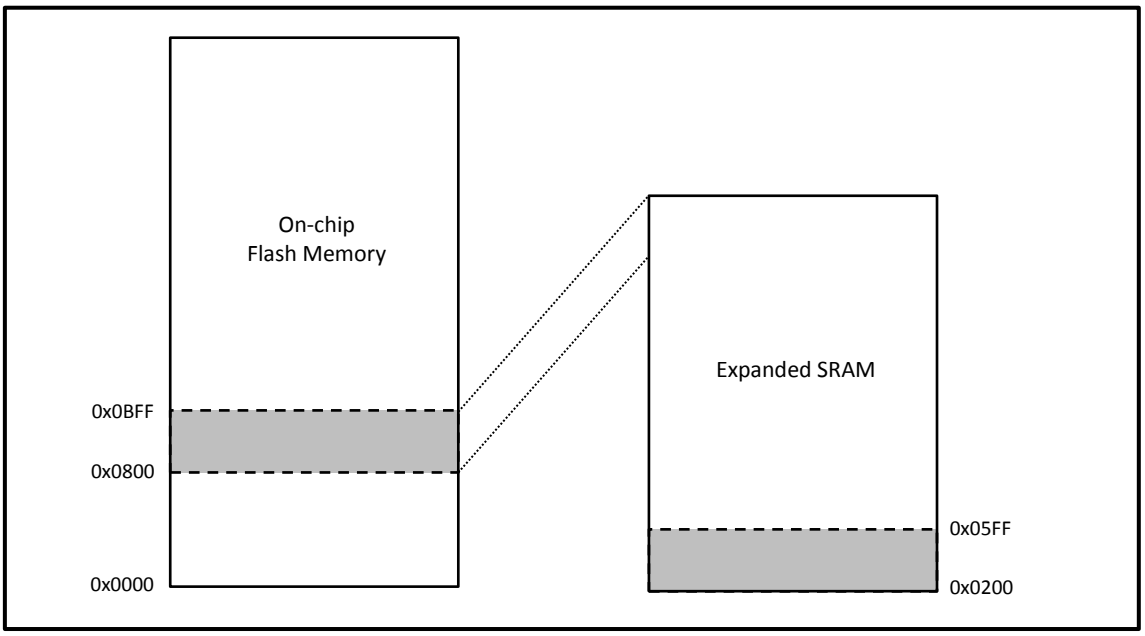
4.1 Program & Data Flash Memory

On-chip program Flash size ranges from 4096 bytes to 30208 bytes, and 64 bytes data Flash are provided for selection upon different application. It can be programmed by In-System-Programming (ISP) method.

In addition, write protection signature is available to avoid writing accidentally.

4.2 Code Executable from SRAM

Code execution enables the mapping of Flash memory to SRAM. This SRAM segment replaces the on-chip Flash memory.



4.3 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, UART, etc. Some locations in the SFR address space are addressable as bits.

4.4 External Function Register (XFR)

The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

5 Architecture

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

Internal RC oscillator is equipped and operated at 12MHz, 8MHz, 6MHz, 4MHz, 2MHz and 1MHz software selectable without external components. It supports trimming by In-System Programmer to ensure the oscillator within specification.

6 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

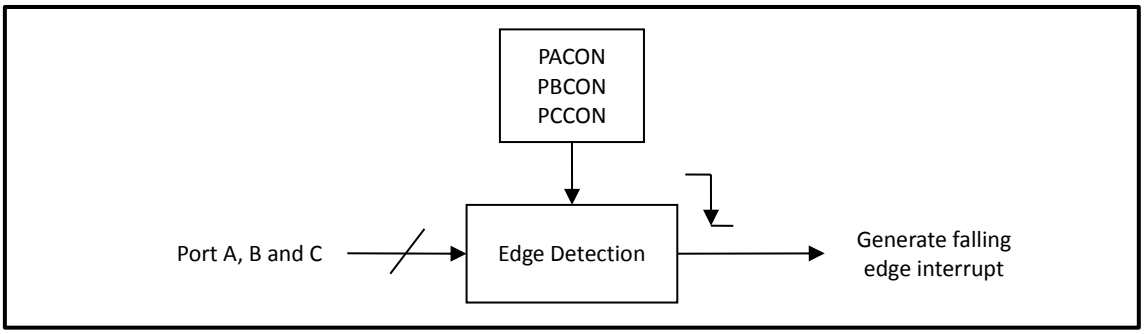
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

7 I/O port

The 20-pin package has one 6-bit port (PA), one 8-bit ports (PB), one 1-bit port (PORTC) and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

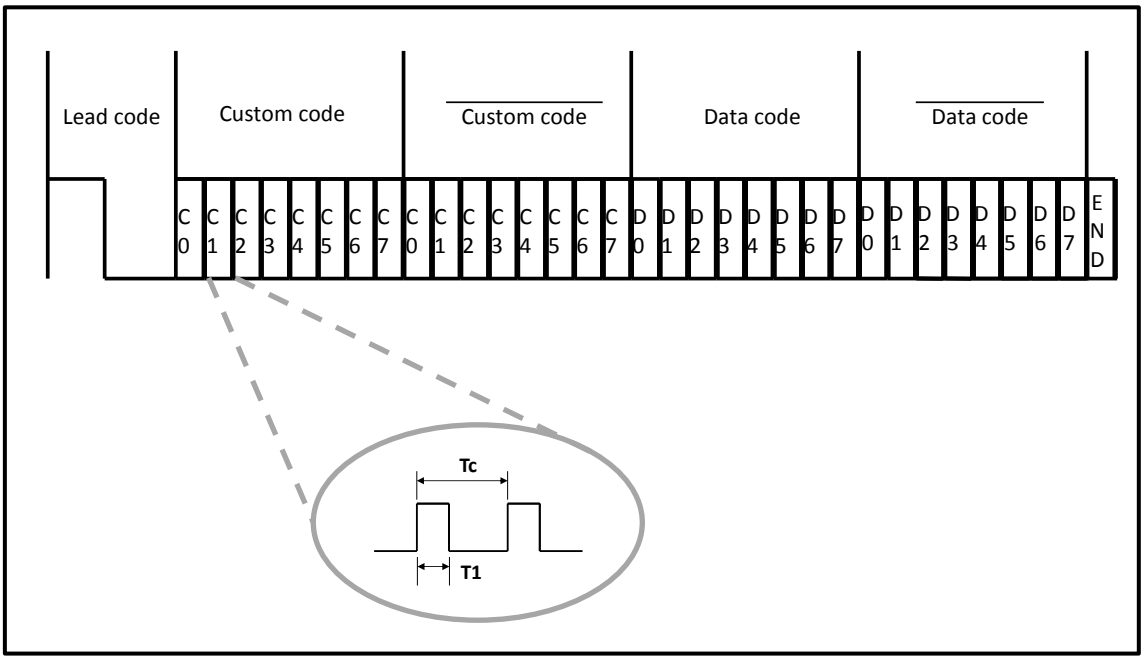
The 24-pin package has two 8-bit ports (PA and PB), one 3-bit port (PORTC), and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

Port interrupt function is supported for port A, B and C. Pull-up resistors are also included and could be assigned pin-by-pin by programming the pull-up resistor enable register.



8 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

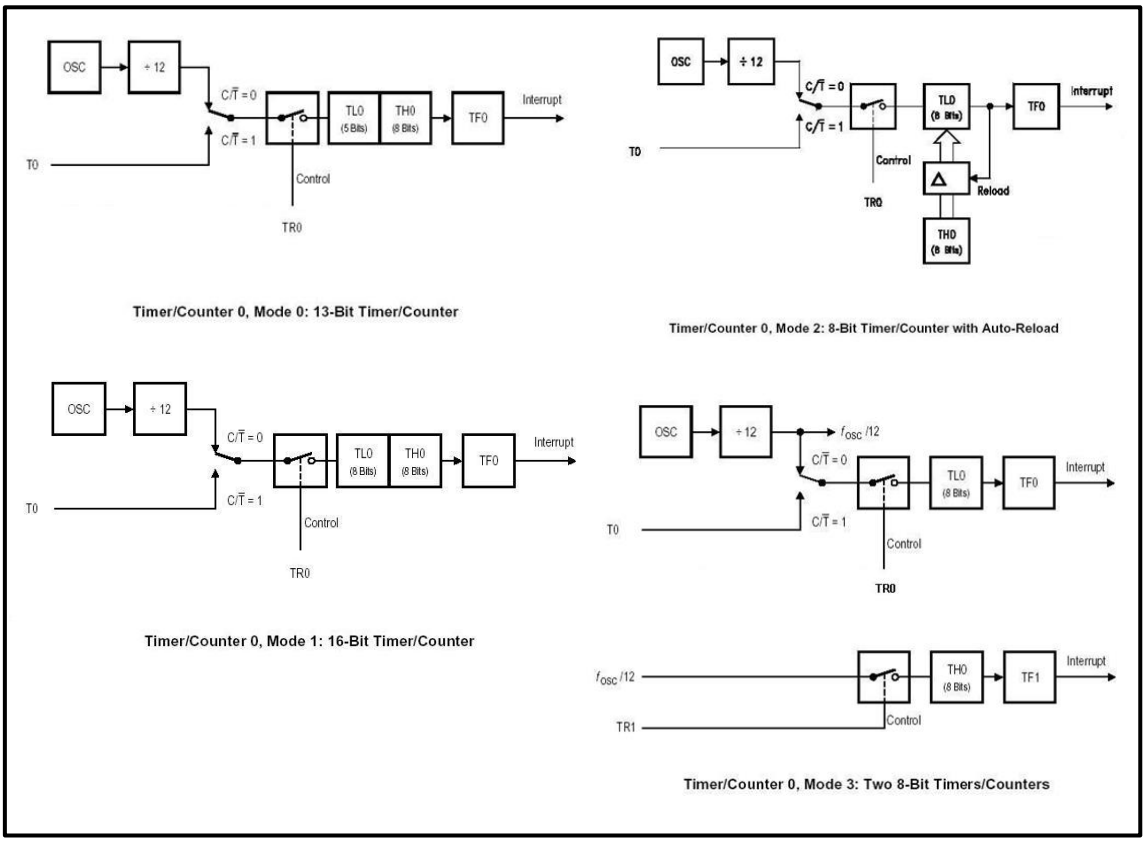
9 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated

for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



10 Enhanced UART

The UART is fully compatible with the standard 8051 serial channel and perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

The full duplex UART ports are able to transmit and receive simultaneously. These serial ports are also receive-buffered. It can commence reception of a second byte before the previously received byte has been read from the receive register.

The UART operates in four modes (one synchronous and three asynchronous). The Serial 0 is buffered at the receive side, i.e. it can receive new data while the previously received is not damaged in the receive register until the completion of the 2nd transfer.

11 Serial Peripheral Interface

SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously. A complete hardware Serial Peripheral Interface (SPI) on-chip in master mode is integrated.

12 Inter-Integrated Circuit (I2C) Interface

The I2C Bus Controller supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: “SCL” (serial clock line) and “SDA” (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus.

The interface defines 2 transmission speeds if 12MHz crystal is used:
- Normal: 100Kbps
- Fast: 400Kbps

The I2C component performs 8-bit-oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode and may operate in the two modes.

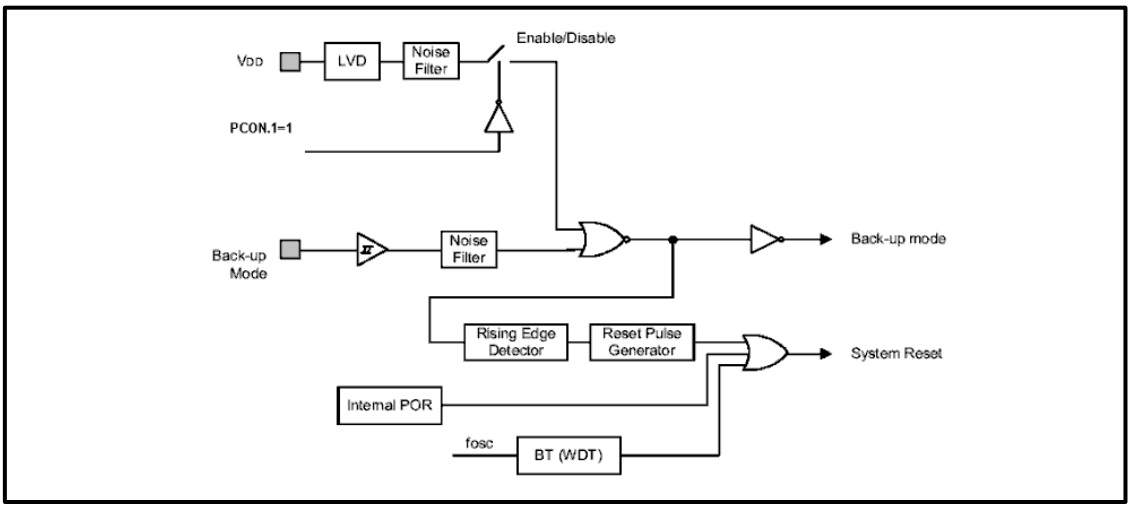
Mode	Description
Master Transmitter Mode	Serial data output through SDA while SCL output the serial clock.
Master Receiver Mode	Serial data is received via SDA while SCL outputs the serial clock.
Slave Receiver Mode [1]	Serial data and the serial clock and received through SDA and SCL
Slave Transmitter Mode [1]	Serial data is transmitted via SDA while the serial clock is input through SCL

13 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



14 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires 6 wires to minimize the number of added components and board area impact.

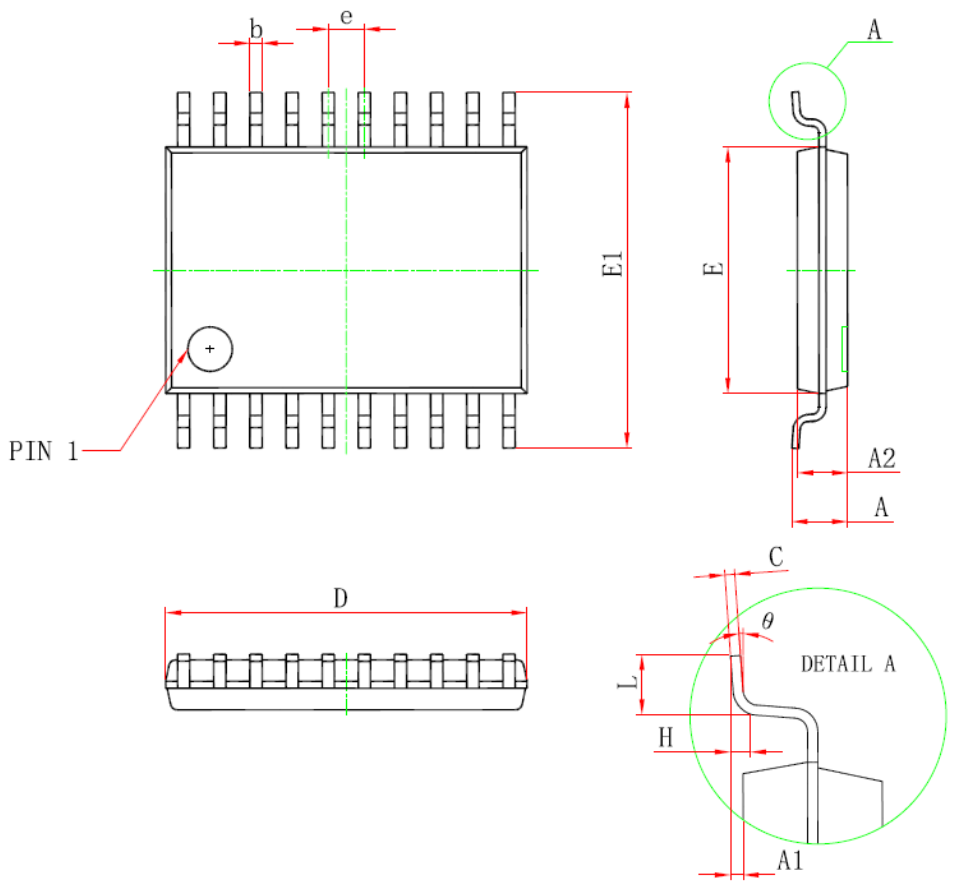
15 Ordering Information

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688F4STT DC6688F4STT-TR1[1]	TSSOP24	4KB	64B	256B + 1.5KB	21
DC6688F16STH DC6688F16STH-TR1[1]	TSSOP20	16KB	64B	256B + 1.5KB	17
DC6688F16STT DC6688F16STT-TR1[1]	TSSOP24	16KB	64B	256B + 1.5KB	21
DC6688F30STH DC6688F30STH-TR1[1]	TSSOP20	30KB	64B	256B + 1.5KB	17
DC6688F30STT DC6688F30STT-TR1[1]	TSSOP24	30KB	64B	256B + 1.5KB	21

[1] Tape and reel packing.

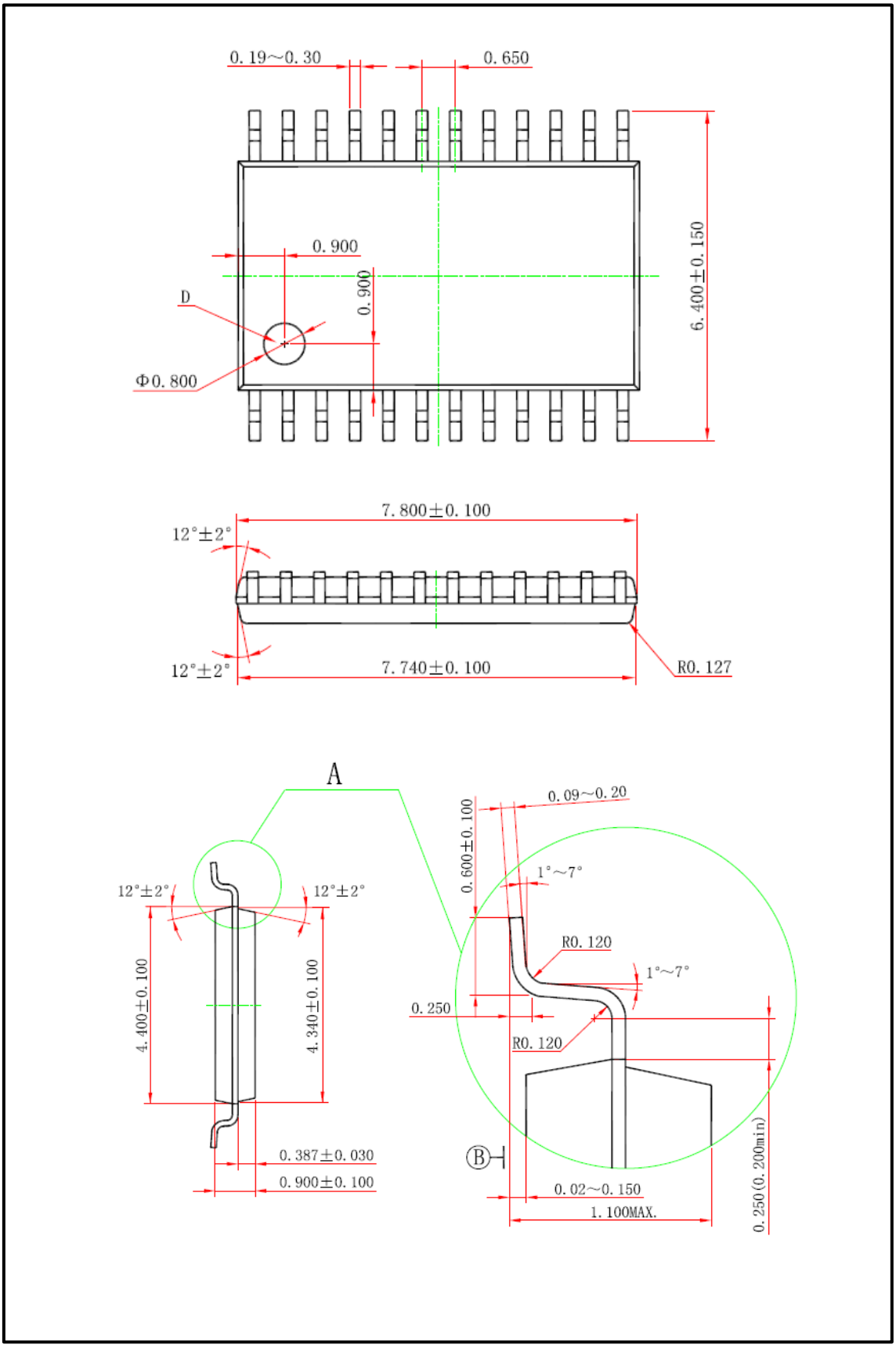
16 Package Outlines

16.1 20-pin TSSOP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

16.2 24-pin TSSOP



17 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	29 Jan, 2014	All	-	New template	Danny Ho	Celia Ki
1.1	17 Apr, 2014	All	-	Change format	Danny Ho	Celia Ki
1.2	30 Apr, 2014	1, 4, 5, 15	-	Add 4KB option	Kennis To	Danny Ho
1.3	5 May, 2014	4, 5, 15	-	Correct typo	Kennis To	Danny Ho
1.4		1.8, 2	-	Remove XIN, XOUT	Danny Ho	Celia Ki
		1, 2, 3, 16.1	-	Added 20-pin TSSOP		
1.5	22 Jul, 2014	1	-	Revise operating temperature and LVD level	Kennis To	Danny Ho
1.6	25 Jul, 2014	1, 15	-	Revise stop mode current spec Added DC6688F16STH	Kennis To	Fred Law
1.7	14 Aug, 2014	All	-	Revise 20-pin TSSOP assignment	Kennis To	Danny Ho
1.8	18 Mar, 2016	All	-	Revise expanded SRAM size	Kennis To	Danny Ho
1.9	Jun, 2017	All	-	Revise information	Patrick Li	
2.0	Jan, 2018	All	-	Revise information	Patrick Li / Kennis To	Kennis To

Copyright Notice

Disclaimer

Dragonchip Ltd. assumes no responsibility for any errors contained herein.

Dragonchip Ltd.
TEL: (852) 2776-0111
FAX: (852) 2776-0996
http://www.dragonchip.com