DC6688WF

Wifi Low-Power Single-Band 802.11 b/g/n MCU

DC6688WF is a low-power Wifi connectivity MCU suitable for IoT application. It is manufactured in advanced CMOS process with 32-bit RISC CPU core and peripherals suitable for low-power IoT device. The embedded Wifi engine can support all mandatory IEEE 802.11 b/g/n data rates and guard interval. DC6688WF has additional LDO and DC-DC buck converter that could provide noise isolation for digital and analog voltage supplies and excellent power efficiency with minimum BOM cost.

Features

- MAC features
  - Support all IEEE 802.11b data rates of 1, 2, 5.5, and 11Mbps
  - Support all IEEE 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
  - Support all IEEE 802.11n MCS0-MCS7, HT20/HT40, 800ns and 400ns guard interval
  - Advanced 1T1R 802.11n features:
    - Full / Half Guard interval
    - Frame Aggregation
    - Reduced Inter-frame Space (RIFS)
    - Space Time Block Coding (STBC)
    - Greenfield mode
  - Soft-AP / STA / Soft-AP + STA mode
  - Security
    - WEP / TKIP / WPA / WPA2
  - Support AT-command control
- High performance 32-bit RISC processor
  - Built-in 128KB ROM and 192KB SRAM for instruction and data
  - 8KB retention SRAM
- Flash controller
  - Supports both flash and PSRAM up to 16MB
- I/O Ports and Communication Channels
  - 22 configurable GPIOs
  - USB 2.0
  - PWM x 5
  - UART that supports baud rate up to 921600bps
  - High-speed UART that supports RTSN/CTSN/RX/TX, baud rate up to 4.8MHz
  - I2C Master
  - I2S Tx/Rx channel for 12-32bit/8-96kHz in master/slave mode
- Operating voltage: 2.1V to 3.5V
- Operating temperature: -20°C to +85°C
- Package type:
  - 48 QFN (6x6mm 0.4mm pitch)

Quick look on Ordering Information

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

The absolute maximum ratings indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Symbol	Description	Max Rating	Unit
VDD16	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD33SX	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33RF	VDD input for RF	-0.3 to 3.6	V
DVDDIO1/3	VDD input for GPIO pins	-0.3 to 3.6	V
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16DC	VDD input for digital circuit's LDO	-0.3 to 3.6	V
VDD33DC	VDD input for DC-DC	-0.3 to 3.6	V
VDD33USB	VDD input for USB	-0.3 to 3.6	V

1.2 Environmental Ratings

Characteristic	Conditions/Comments	Value	Unit
Ambient Temperature (T_A)	Functional operation	-20 to 85	^oC

1.3 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168-hours of factory conditions < 30 °C /60%RH
b) Storage humidity needs to maintained at <10% RH
c) Baking is necessary if customer exposes the component to air over 168 hrs, baking condition: 125°C / 8hrs

1.4 Thermal Characteristics

Thermal characteristics without external heat sink in still air condition.

Symbol	Description	Typ	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	^oC
θ_{JA}	Thermal Resistance θ_{JA} ($^oC/W$) for JEDEC 4L System PCB	37.8	$^oC/W$
θ_{JC}	Thermal Resistance θ_{JC} ($^oC/W$) for JEDEC 4L System PCB	TBD	$^oC/W$
ΨJt	Thermal Characterization parameter ΨJt (°C /W) for JEDEC 4L system PCB	4.13	$^oC/W$
	Maximum Lead Temperature (Soldering 10s)	260	^oC

Notes: * JEDEC 51-7 system FR4 PCB size: 3" x 4.5" (76.2 x 114.3 mm)

* Thermal characteristics without external heat sink in still air condition

1.5 Electrostatic Discharge Specifications

This is an ESD sensitive product! Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Pin Type	Test Condition	Value	Unit
Human Body Mode (HBM)	MIL-STD-883G Method 3015.7	Passed ±2.5	kV
Charged Device Model (CDM)	JEDEC -500 +500V Specification JESD22-C101, all pins	Passed ±500	V

1.6 Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VDD16	VDD input for analog 1.6V		1.6		V
VDD33SX	VDD input for external components I/O control	2.1	3.3	3.46	V
VDD33RF	VDD input for RF	2.1	3.3	3.46	V
DVDDIO1/3	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16DC	VDD input for digital circuit's LDO		1.6		V
VDD33DC	VDD input for DC-DC	2.1	3.3	3.46	V
VDD33USB	VDD input for USB	3.13	3.3	3.46	V

1.7 DC Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage when VDDIO=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage when VDDIO=3.3V	2		3.6	V
V_{T+}	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.6	1.74	1.89	V
V_{T-}	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.27	1.4	1.56	V
V_{OL}	Output low voltage when VDDIO=3.3V			0.4	V
V_{OH}	Output high voltage when VDDIO=3.3V	2.4			V
R_{PD}	Input weak pull-down resistance when VDDIO=3.3V		TBD		kΩ
R_{PU}	Input weak pull-high resistance when VDDIO=3.3V		TBD		kΩ
I_{OL}	Low level output current @V_{OL}(max), 8mA setting	11.9	17.7	23.4	mA
	Low level output current @V_{OL}(max), 12mA setting	15.8	23.5	31.1	mA
I_{OH}	High level output current @V_{OH}(min), 8mA setting	17.2	34.1	58.8	mA
	High level output current @V_{OH}(min), 12mA setting	23.9	47.2	81.5	mA

1.8 Crystal Oscillator Specifications

Parameter	Conditions / Notes	Min.	Typ.	Max.	Unit
Frequency Range	-	Between 19.2MHz and 52MHz			
Crystal Load Capacitance	-	9	-	11	pF
ESR	-	-	-	50	Ω
Frequency tolerance over operating temperature	-	-20	-	20	ppm

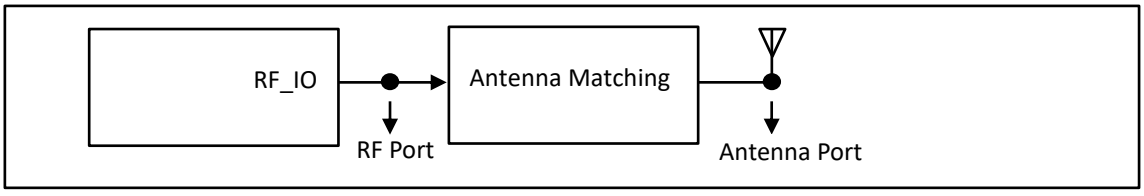
1.9 External Clock-Requirements and Performance

Parameter	Conditions / Notes	Min.	Typ.	Max.	Unit
Frequency Range	-	Between 19.2MHz and 52MHz			
OSCIN Input Voltage	AC-couple analog signal	-400	-	1500	mV_{PP}
Frequency tolerance Initial and over temperature	-	-20	-	20	ppm
Duty Cycle	26MHz	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1kHz offset	-	-	-119	dBc/Hz
	26MHz clock at 10kHz offset	-	-	-129	dBc/Hz
	26MHz clock at 100kHz offset	-	-	-134	dBc/Hz
	26MHz clock at 1MHz offset	-	-	-139	dBc/Hz
Phase Noise(802.11n 2.4GHz)	26MHz clock at 1kHz offset	-	-	-125	dBc/Hz
	26MHz clock at 10kHz offset	-	-	-135	dBc/Hz
	26MHz clock at 100kHz offset	-	-	-140	dBc/Hz
	26MHz clock at 1MHz offset	-	-	-145	dBc/Hz

1.10 WLAN RF Performance Specifications

Parameter	Conditions / Notes	Min.	Typ.	Max.	Unit
Frequency Range	-	2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1Mbps	-	-95.5	-	dBm
	CCK, 2Mbps	-	-93.5	-	dBm
	CCK, 5.5Mbps	-	-91.0	-	dBm
	CCK, 11Mbps	-	-88.0	-	dBm
Rx Sensitivity (OFDM)	OFDM, 6Mbps	-	-91.5	-	dBm
	OFDM, 9Mbps	-	-90.0	-	dBm
	OFDM, 12Mbps	-	-88.0	-	dBm
	OFDM, 18Mbps	-	-86.0	-	dBm
	OFDM, 24Mbps	-	-82.5	-	dBm
	OFDM, 36Mbps	-	-79.5	-	dBm
	OFDM, 48Mbps	-	-74.5	-	dBm
	OFDM, 54Mbps	-	-73.5	-	dBm
Rx Sensitivity (HT20) Greenfield 800ns GI Non-STBC	HT20, MCS0	-	-91.0	-	dBm
	HT20, MCS1	-	-88.0	-	dBm
	HT20, MCS2	-	-86.0	-	dBm
	HT20, MCS3	-	-81.5	-	dBm
	HT20, MCS4	-	-79.0	-	dBm
	HT20, MCS5	-	-74.5	-	dBm
	HT20, MCS6	-	-73.5	-	dBm
	HT20, MCS7	-	-72.5	-	dBm
Rx Adjacent Channel Rejection (CCK)	CCK, 1Mbps (30MHz offset)	-	41	-	dB
	CCK, 11Mbps (25MHz offset)	-	41	-	dB
Rx Adjacent Channel Rejection (OFDM)	OFDM, 6Mbps (25MHz offset)	-	39	-	dB
	OFDM, 54Mbps (25MHz offset)	-	23	-	dB
Rx Adjacent Channel Rejection (HT20)	HT20, MCS0 (25MHz offset)	-	38	-	dB
	HT20, MCS7 (25MHz offset)	-	21	-	dB
Tx Output Power	CCK, 1-11Mbps	-	19	-	dBm
	OFDM, 54Mbps	-	16	-	dBm
	HT20, MCS7	-	15	-	dBm

Note: All specifications are measured at the antenna port unless otherwise specified.



1.11 Power Consumption at DCDC mode (DCDC buck convertor is enabled)

WLAN Operational Modes	Typ.	Unit
OFF[a]	2	uA
Rx, CCK, 1Mbps	68	mA
Rx, OFDM, 54Mbps	68	mA
Rx, HT20, MCS7	68	mA
Rx, HT40, MCS7	75	mA
Tx, CCK, 1Mbps	307	mA
Tx, OFDM, 54Mbps @ 15dBm	256	mA
Tx, HT20, MCS7 @ 15dBm	260	mA
Tx, HT40, MCS7 @ 15dBm	260	mA
Power-saving (MCU on)[b], DTIM1	27	mA
Power-saving (MCU on)[b], DTIM3	26.5	mA
Power-saving (MCU off)[c], DTIM1	1.8	mA
Power-saving (MCU off)[c], DTIM3	1.1	mA

1.12 Power Consumption at LDO mode (DCDC buck convertor is disabled)

WLAN Operational Modes	Typ.	Unit
OFF[a]	2	uA
Rx, CCK, 1Mbps	113	mA
Rx, OFDM, 54Mbps	113	mA
Rx, HT20, MCS7	124	mA
Tx, CCK, 1Mbps @ 18dBm	328	mA
Tx, OFDM, 54Mbps @ 15dBm	280	mA
Tx, HT20, MCS7 @ 15dBm	283	mA
Tx, HT40, MCS7 @ 15dBm	285	mA
Power-saving (MCU on)[b], DTIM1	38.5	mA
Power-saving (MCU on)[b], DTIM3	38	mA
Power-saving (MCU off)[c], DTIM1	2.6	mA
Power-saving (MCU off)[c], DTIM3	1.5	mA

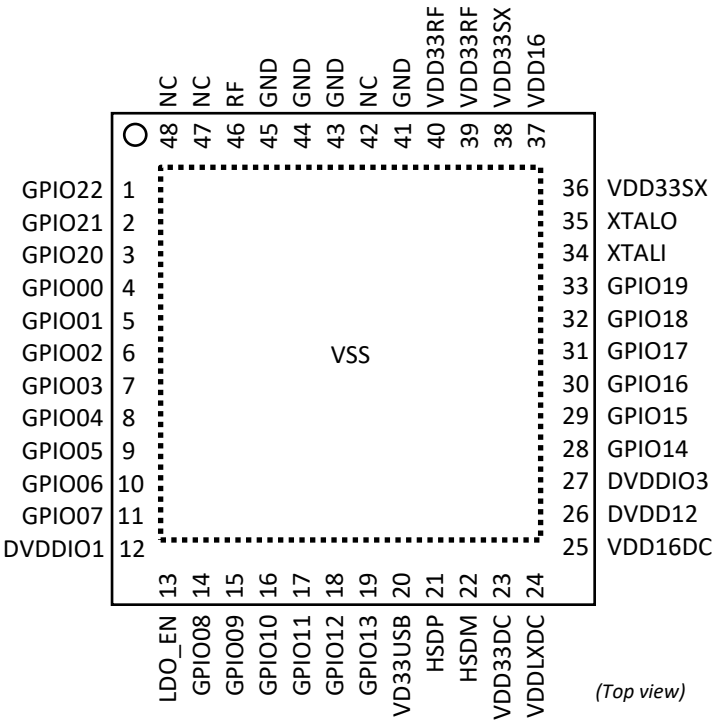
Note: a. OFF mode test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V (excluding PSRAM/flash).

b. Intra-beacon Sleep when MCU is turn on.
It is used in the applications that require the CPU to be working.

c. Intra-beacon Sleep when MCU is turn off.

2 Pin Assignment

QFN48



(Top view)

2.1 Power Pins

Pin No.	Pin	Function	Decoupling
12	DVDDIO1	3.3V VDD supply for I/O	1uF
20	VDD33USB	3.3V VDD supply for USB	
23	VDD33DC	3.3V analog input for DC-DC	1uF
24	VDDLXDC	DC-DC buck regulator: output to inductor	4.7uH + 4.7uF
25	VDD16DC	DC-DC 1.6V	4.7uH + 4.7uF
26	DVDD12	Digital 1.2V input	1uF
27	DVDDIO3	3.3V VDD supply for I/O	1uF
36	VDD33SX	Analog 3.3V input	1pF
37	VDD16	Analog 1.6V input	1uF
39,40	VDD33RF	3.3V VDD supply for RF	2.2uF
41,43-45	GND	Ground pin	

2.2 Special Pins

Pin No.	Pin	Function	Remarks
13	LDOEN	Reset signal to power-down IC	When this signal is low, the chip will enter off mode. This pin can be used to reset the chip.
34,35	XTALI, XTALO	Input/Output of crystal clock	
46	RF	2.4GHz RF input/output port	

2.3 Bootstrap Conditions

DC6688WF has 3 bootstrapping pins to select I/O interface for SPI flash/PSRAM mode or USB 2.0 (for firmware upgrade only) mode. Please refer to the table below for the settings of GPIO15, GPIO14, and GPIO07 during bootstrapping.

GPIO15,GPIO14, GPIO07	Interface Mode
000	SPI Flash/PSRAM mode (default) (for firmware storage only)
110	USB 2.0 mode (for firmware upgrade only)

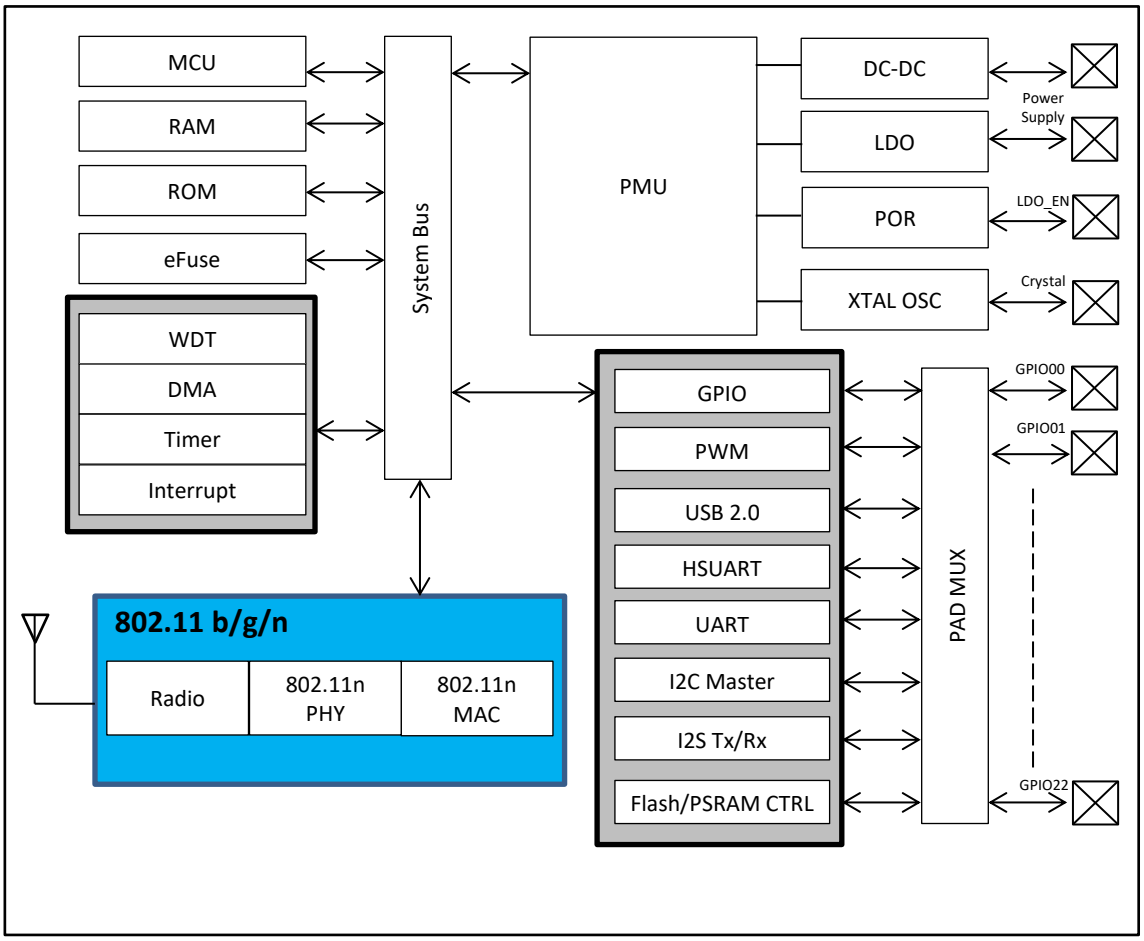
2.4 GPIO settings for SPI Flash/PSRAM Interface

Please refer to the following GPIO settings when [GPIO15,GPIO14,GPIO07]=000 during bootstrapping.

Pin No.	Pin	I/O	PU/PD	I/O Function
4	GPIO00	I/O	-	-
5	GPIO01	I	-	-
6	GPIO02	I	PU	-
7	GPIO03	I	-	UART0_RXD
8	GPIO04	O	-	UART0_TXD
9	GPIO05	O	-	UART1_RTS
10	GPIO06	I	-	UART1_RXD
11	GPIO07	O	PU	UART1_TXD
14	GPIO08	I/O	-	GPIO08
15	GPIO09	I	-	UART1_CTS
16	GPIO10	I/O	-	GPIO10
17	GPIO11	I/O	-	GPIO11
18	GPIO12	I/O	-	GPIO12
19	GPIO13	O	PU	SPI_PSRAM_CSN
28	GPIO14	I/O	PD	SPI_FLASH_IO0_DI (MOSI)
29	GPIO15	O	PD	SPI_FLASH_CLK
30	GPIO16	I/O	PU	SPI_FLASH_IO3_HD
31	GPIO17	O	PU	SPI_FLASH_CSN
32	GPIO18	I/O	PD	SPI_FLASH_IO1_DO (MISO)
33	GPIO19	I/O	PU	SPI_FLASH_IO2_WP
3	GPIO20	I/O	-	GPIO20
2	GPIO21	I	-	I2C_S_SCL
1	GPIO22	I/O	-	I2C_S_SDA

3 System Overview

The DC6688WF is designed to support IEEE 802.11 b/g/n single stream with the state of the art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The DC6688WF WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The DC6688WF WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.



3.1 MAC Features

- 802.11 b/g/n/e/i/d
- WLAN/BT coexistence mechanisms
- 802.11n features
  - A-MPDU Tx & Rx
  - Support immediate Block-Ack
- Soft-AP / STA / Soft-AP + STA mode
- Rate adaption mechanism
- WFA features
  - WEP/TKIP/WPA/WPA2
  - WMM/WMM PS

3.2 PHY Features

- 802.11b, 11g, and 802.11n 1T1R
- Short Guard Interval
- Greenfield mode
- RIFS in RX mode
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

3.3 System

- 32-bit RISC processor w/ ILM/DLM and I-cache.
- 128K ROM and 192 KB SRAM for Instruction and data SRAM in total.
- 8K retention SRAM.
- Suspend/Wake-up manger controller.
- Two channel DMA off load CPU loading.
- One Flash controller supports both Flash and PSRAM up to 16MB with XIP.
- One I2S TX/RX channel for 12~32bits/8~96KHz in master/slave mode.
- One I2C master
- Five PWMs
- Four millisecond timers
- Four microsecond timers
- Two watchdog
- All pins can be multiplexed to GPIO by user scenario

3.4 Host Interface

- USB 2.0 (only valid when [GPIO15,GPIO14]=11 during bootstrap) (for firmware upgrade only)
- High Speed UART
    - Support RTSN/CTSN/RX/TX, 4 pins
    - Baud rate up to 4.8MHz
- UART
    - Support RX/TX, 2 pins
    - Baud rate up to 921600

3.5 System Clocking and Reset

The DC6688WF has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

3.6 Design for Test

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

4 Power Supply Management

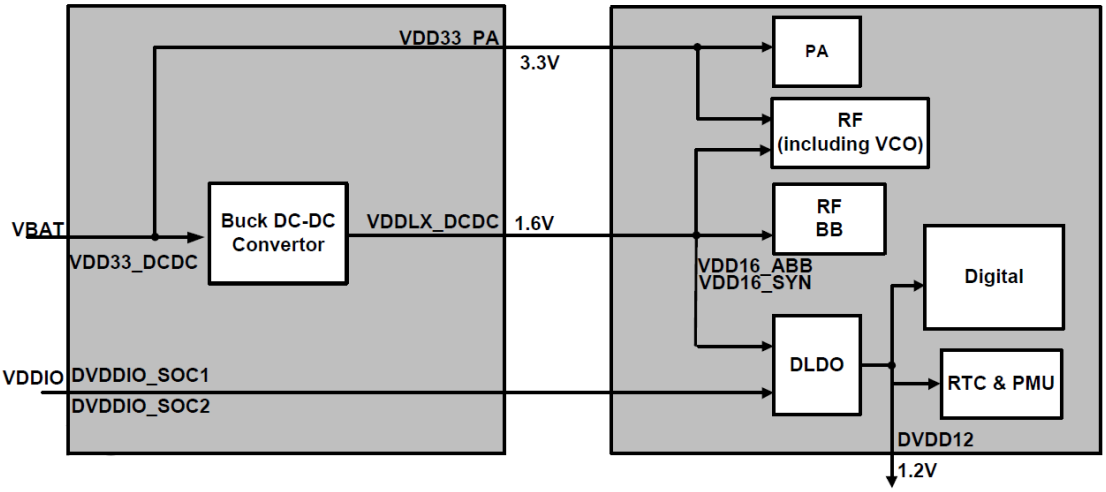
4.1 Power Consumption at LDO mode (DCDC buck convertor is disabled)

The power management unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrated multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.6V and feeds into the input power of the RF circuit and DLDO which has 1.2V output voltage for all digital circuits.

Below figure shows the typical power connection for DC6688WP. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 1.8V or 3.3V from the host side. The connection structure is shown in the figure below.



4.2 Under-Voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the battery is below pre-defined threshold. It ensures that DC6688WF is powered on with the battery in good condition. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself to prevent further discharging.

4.3 DLDO

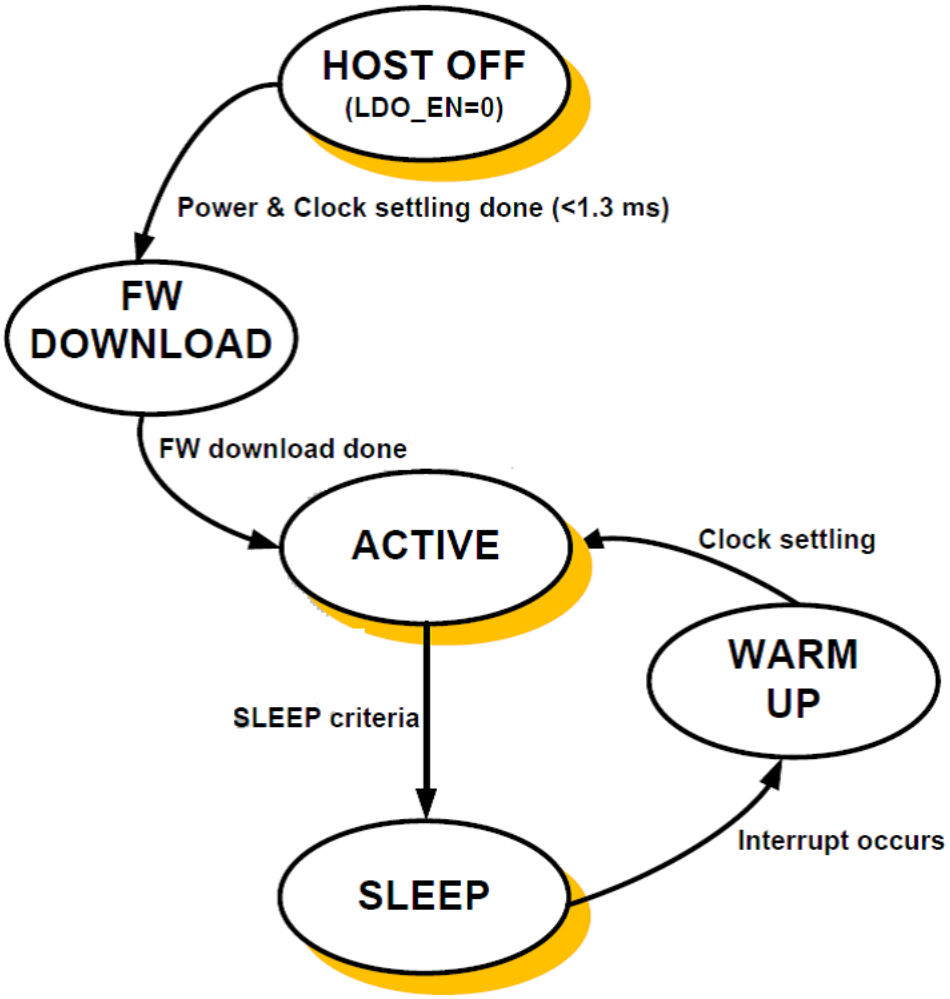
The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.6V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

4.4 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.5V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

4.5 Power Management Control

There are three power modes that DC6688WF operates when it is initialized: HOST_OFF, ACTIVE mode and SLEEP mode. There are two intermediate system transition modes: FW_DOWNLOAD and WARM_UP mode. The following are the brief introduction to each mode



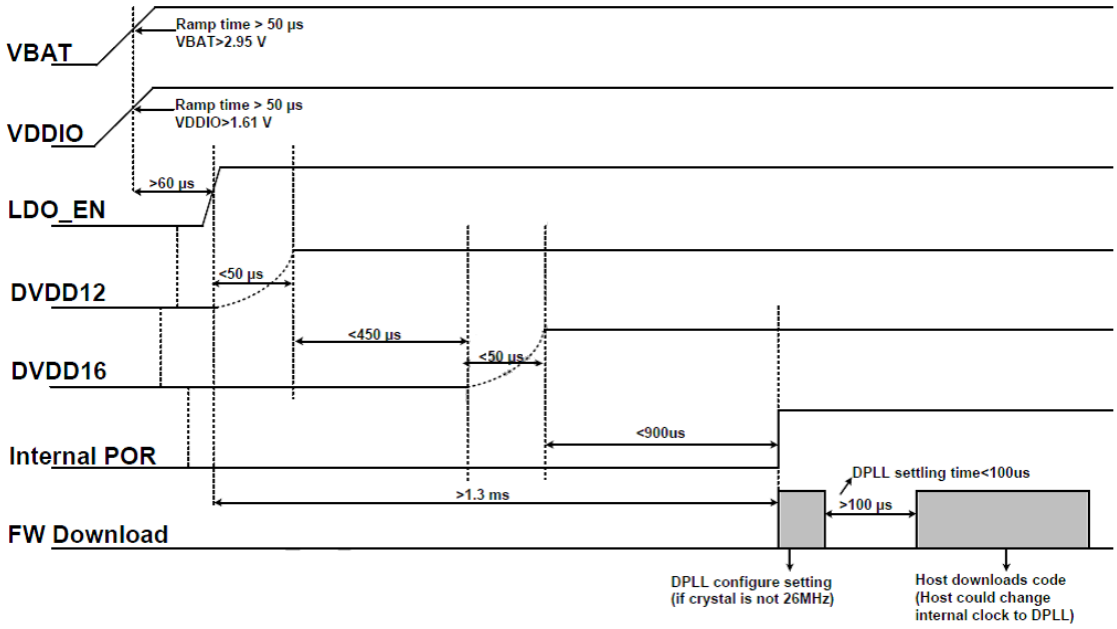
State	Description
HOST OFF	When **LDO_EN** pin is de-asserted and logically low, the chip is brought to this state immediately.
	Sleep clock and internal power supply is disabled.
	After LDO_EN pin is asserted, the internal power and clock will be settled down within 1.3 ms.
FW DOWNLOAD	States for firmware download after power and clock is settled down.
SLEEP	The host controller can determine when to enter sleep to turn off most circuit in DC6688WF. All the RF, DPLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.
	All internal states are maintained and the Crystal oscillator is disabled.
WARM UP	The system transitions from SLEEP to ACTIVE. The crystal or oscillator is brought up and the PLL is enabled.
ACTIVE	The high speed clock is operational and sent to each block by the clock control register.
	The RF circuit is enabled to transmit or receive data, and the whole system is under normal operation.

4.6 Power-On Sequence

Below figure shows the power-on sequence of the DC6688WF from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the DC6688WF or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the DC6688WF. From that point, the typical DC6688WF power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.

2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.



4.7 Reset Control

The DC6688WF LDO_EN pin can be used to completely reset the entire chip. After this signal has been de-asserted, the DC6688WF is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the DC6688WFP turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

5 25MHz Crystal Selection Guide

For the best performance across the lifetime of the application, we recommended the following crystal parts.

Manufacturer	Prod. Code	Package	ESR (Ω)	CL (pF)	Tolerance (ppm)	Aging (ppm/Year)	Temp. Range (℃)
Hong Kong X'tals Limited	HKC3225SX-25MHz-28234-R4V1	3225	50	9	15	5	-40 85

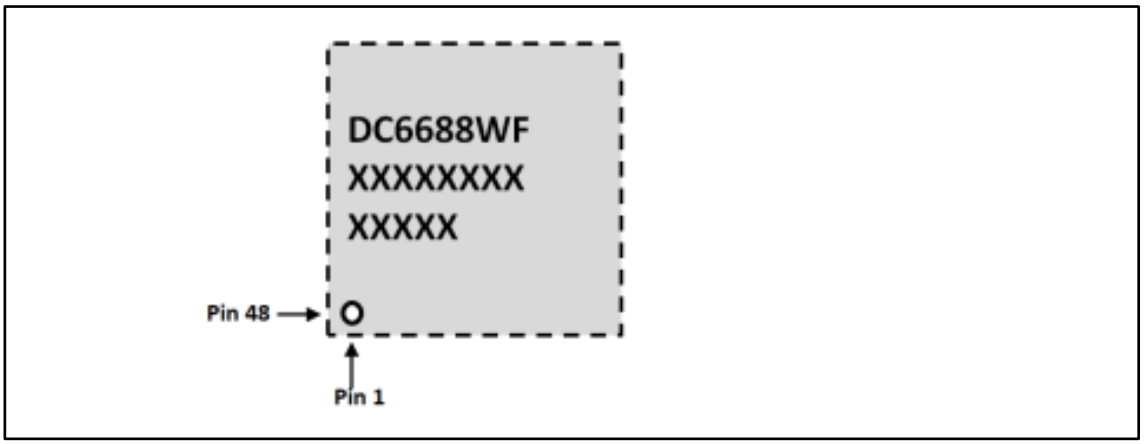
6 Ordering Information

Part No	Package
DC6688WF	QFN48

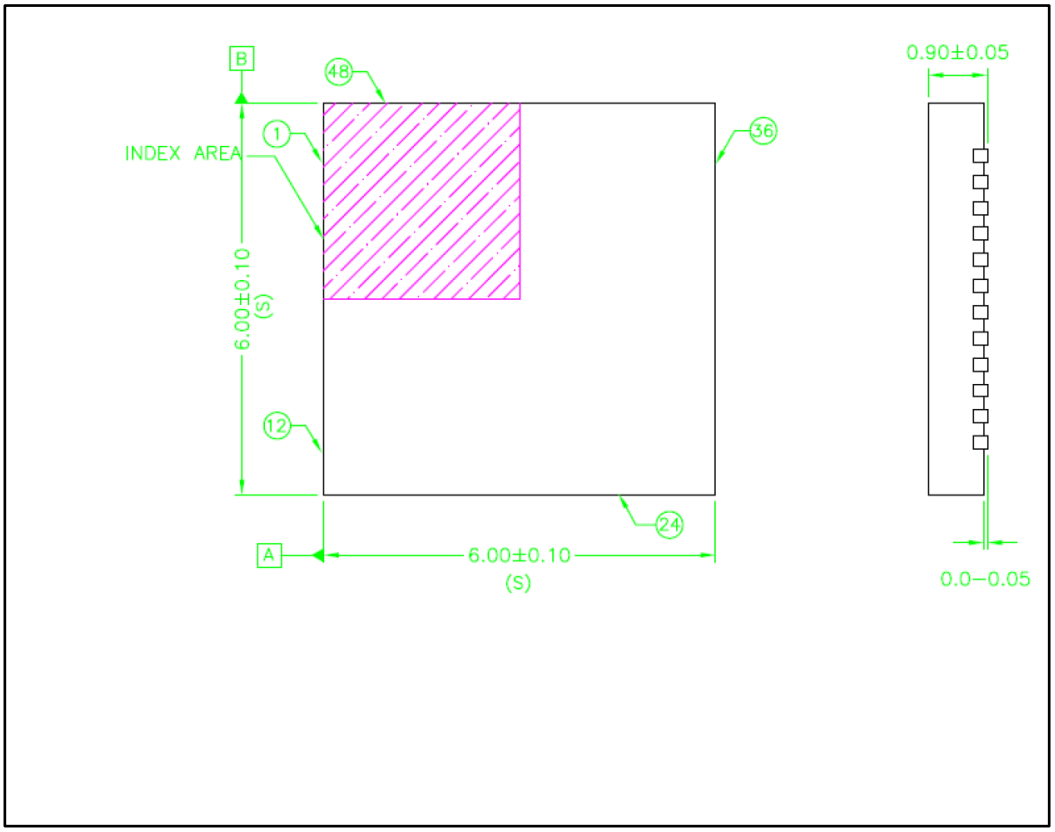
7 Package Outlines

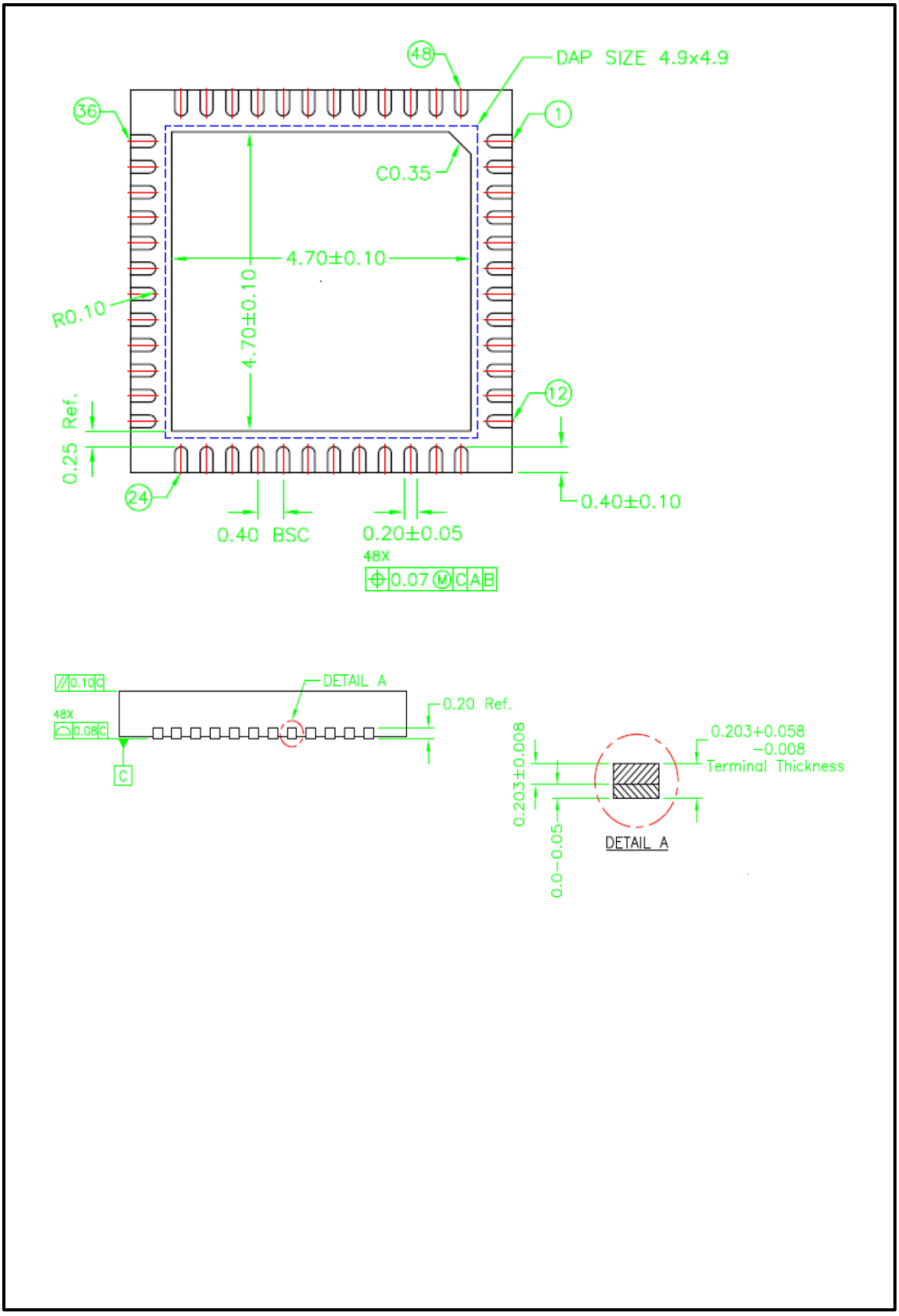
7.1 48-pin QFN

6 x 6 mm (body size), 0.4mm pitch, QFN48
Marking format (top-view)



Package Dimensions




48
DAP SIZE 4.9x4.9
36
1
C0.35
4.70±0.10
4.70±0.10
R0.10
12
0.25 Ref.
24
0.40±0.10
0.40 BSC
0.20±0.05
48X
0.07 M C A B
0.10 C
48X
0.08 C
C
DETAIL A
0.20 Ref.
0.203±0.008
0.203+0.058
−0.008
Terminal Thickness
0.0−0.05
DETAIL A

8 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	Jun, 2018	-	-	Initial version	Patrick Chan	Fred Law
1.1	Dec, 2018	-	1,11	Changed 16Mb to 16MB	Patrick Chan	Fred Law
1.2	Jan, 2019		5	Changed oscillator load cap. & ESR	Patrick Chan	Danny Ho
1.3	Feb, 2019	5	-	Add section 'crystal selection guide'	Danny Ho	Patrick Chan
1.4	May, 2019	1,2, 3.4	-	Added bootstrap behavior of all IO Modified pin assignment Modified features Modified system overview Modified electrical characteristics	Patrick Chan	Danny Ho

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